Radiation Effects Evaluation of the TPS7H4104-SP Radiation-Hardened, 3V to 7V Input, 3A per Channel, Multichannel, Synchronous Buck Converter

Joel Cruz-Colon, Anthony Marinelarena, Tyler Lew and Andy Fondaw

Texas Instruments, Dallas, TX, USA

joel.cruz@ti.com

Introduction

The TPS7H4104-SP is a monolithic radiation-hardened peak-current-mode, synchronous step-down converter offered in a 64-pin plastic (HTQFP) package. This device contains four identical channels that can be used to step down the input voltage (PVIN) into four independent output voltages up to 3A per channel or paralleled to increase the total output current. Each channel operates 90° out-of-phase relative to other channels. Each channel incorporates high-side and low-side MOSFETs with programmable features per channel:

- Slope Compensation (SCx)
- Soft-Start (SS_TRx)
- Power Good Flag for UV and OV (PWRGDx)
- Enable (ENx)
- External Compensation Pin (COMPx)

In addition to these features the device incorporates current limit protection, over-voltage protection, thermal shutdown and internal power-up sequencing with reverse power-down sequencing. The functional block diagram is presented in Fig. 1. This poster presents the Single-Event-Effects (SEE), Total-Ionizing-Dose (TID), Neutron-Displacement-Damage (NDD) along with a system-level application to regulate the output voltage below the 600mV internal reference.

SEE Test Setup

The TPS7H4104-SP was tested at the Texas A&M Cyclotron Institute using ^{165}Ho (@ 15 MeV/u) and at the Michigan State University (MSU) Facility for Rare Isotope Beams (FRIB) using a linear accelerator (LinAc) with ^{169}Tm (@ 20.3 MeV/u). Both facilities used an incident angle to achieve a Linear Energy Transfer (LET) of 75 MeV·cm^2/mg. SEE testing was performed using the TPS7H4104EVM-CVAL evaluation module with two system-level configurations for V_{OUTx}=1.2V and 1.8V. All channels were configured the same way and a load current of 3A was used for all testing.

Throughout the SEE testing campaign, all channels were operated independently, and the input current was monitored continuously. PWRGD, SS_TR, and VOUT were monitored for transients. Various channels were monitored across the testing campaign to collect a comprehensive spectrum of results. A flux of approximately 10^5 ions·cm^2·mg^{-1}·s^{-1} and a fluence of 10^7 ions·cm^2·mg^{-1} (per run) were used for the test campaign.

SEE Test Results

For Single-Event-Latchup (SEL), Single-Event-Burnout (SEB), and Single-Event-Gate-Rupture (SEGR), the maximum recommended voltage stress of 7V was used. For SEL testing, the junction temperature was set to 125°C, while SEB/SEGR and SET testing were conducted at room temperature. SEB/SEGR testing was conducted with the device both enabled and disabled. No abnormal current fluctuations were observed during the entire SEE test campaign. Typical supply current plots for SEL and SEB/SEGR are presented in Figure 2 and Figure 3, respectively. SET testing was conducted at PVIN = 3.3V to VOUTx = 1.2V and PVIN = 5V to VOUTx = 1.8V. Not a single transient was recorded using a window trigger set to ±3% on VOUTx and -20% falling edge trigger on SS_TRx and PWRGDx. SEE summary and upper-bound cross-sections are shown in Table I and Table II.

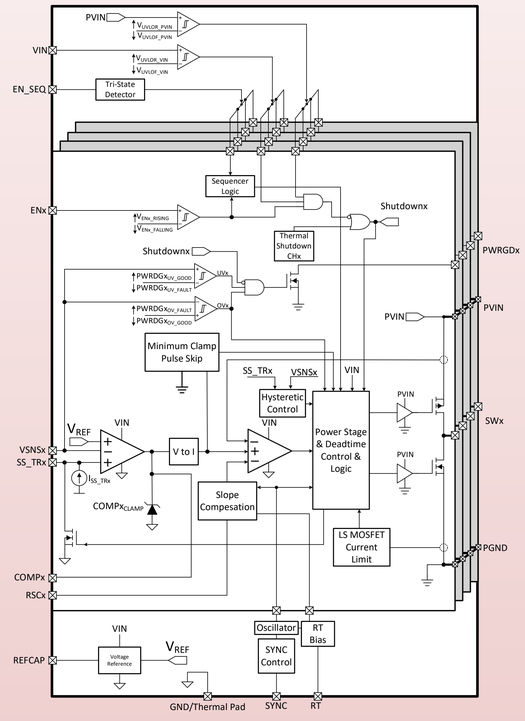


Fig. 1 Functional Block Diagram

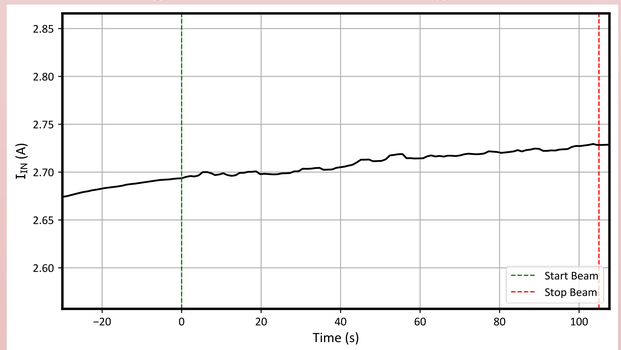


Fig. 2 SEL (V_{OUTX} = 1.2V) Current vs. Time for PVIN and VIN Supply

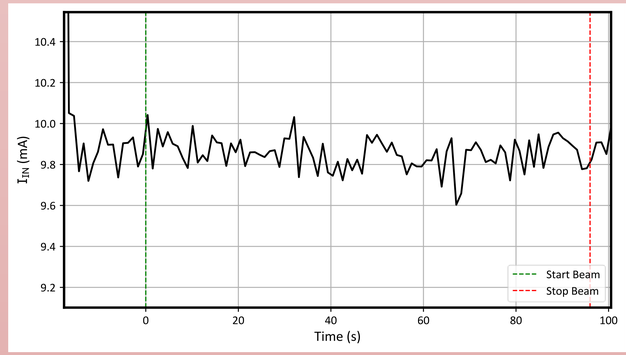


Fig. 3 SEB/SEGR (Disabled) Current vs. Time for PVIN and VIN Supply

Table I. SEL and SEB/SEGR Test Summary

Test Type	Facility	Ion	$V_{OUT\,x}$(V)	Average Flux (ions·cm^{-2}·s^{-1})	Cumulative Fluence (ions·cm^{-2})	Pass?
SEL	TAMU	^{165}Ho	1.2	7.69 x 10^4	4.00 x 10^7	Yes
			1.8	8.13 x 10^4	4.00 x 10^7	Yes
	MSU	^{169}Tm	1.2	1.11 x 10^5	2.00 x 10^7	Yes
			1.8	1.03 x 10^5	2.00 x 10^7	Yes
SEB/SEGR	TAMU	^{165}Ho	1.2	5.89 x 10^4	2.00 x 10^7	Yes
			1.8	5.44 x 10^4	2.00 x 10^7	Yes
			Disabled	5.40 x 10^4	4.00 x 10^7	Yes
	MSU	^{169}Tm	1.2	1.20 x 10^5	1.00 x 10^7	Yes
			1.8	1.05 x 10^5	1.00 x 10^7	Yes
			Disabled	1.14 x 10^5	2.00 x 10^7	Yes

Table II. SET Test Summary

Test Type	Facility	Ion	Average Flux (ions·cm^{-2}·s^{-1})	Cumulative Fluence (ions·cm^{-2})	PVIN (V)	V_{OUTx} (V)	V_{OUTx} SET (#)	PWRGDx SET (#)	SS_TRx SET (#)
SET	TAMU	^{165}Ho	7.71 x 10^4	4 x 10^7	3.3	1.2	0	0	0
			7.70 x 10^4	4 x 10^7	5	1.8	0	0	0
	MSU	^{169}Tm	1.13 x 10^5	2 x 10^7	3.3	1.2	0	0	0
			1.05 x 10^5	2 x 10^7	5	1.8	0	0	0

TID and NDD

The TPS7H4104-SP was tested according to MIL-STD-883:

- Test Method 1019.9 using Condition A for HDR and D for LDR
- Test Method 1017 (as a guidance) for NDD

This device was tested up to the radiation lot acceptance testing (RLAT) level of 100 krad (Si) for TID and up to 10^{13} neutrons/cm^2 for NDD. High Dose Rate (HDR) and Low Dose Rate (LDR) exposure was performed with biased and unbiased units. HDR was conducted on a ^{60}Co gamma cell irradiator located at a Texas Instruments (TI) facility in Dallas, TX. The unattenuated dose rate for the HDR cell was 171 rad (Si)/s. LDR was conducted at RTS with a dose rate of 10mrad (Si)/s. The NDD was conducted at the University of Massachusetts Lowell. After exposure, all units were packed in dry ice (only for TID) and tested using the production automated test (ATE) program. All devices were fully functional and remained within electrical specifications after the exposure. Figs. 4 and 5 show two key specifications — internal voltage reference and high-side switch overcurrent threshold — performance against 50 krad and 100 krad HDR levels

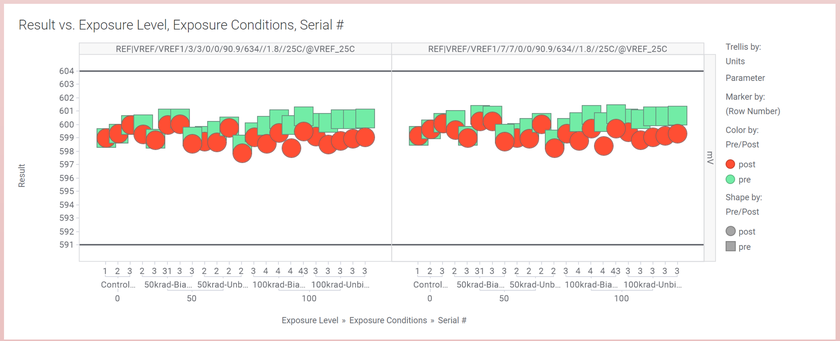


Fig. 4 Internal Voltage Threshold Performance vs HDR levels

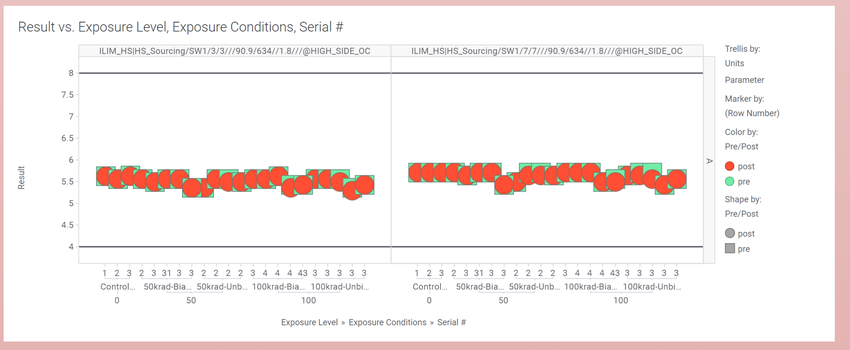
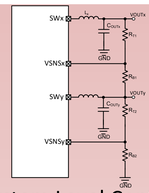


Fig. 5 High-side Switch Overcurrent Threshold vs. HDR levels

System Level Configuration for $V_{OUTx} < V_{REFx}$

The TPS7H4104 has an internal reference of 600mV. When lower output voltages are needed, any of the device channels can be used to create an offset on the feedback pin to effectively achieve lower output voltages than the internal references in any desired channel. By configuring two channels as shown in Fig. 6 the system can achieve regulation below the internal reference. The Equation to calculate the output voltage is shown in equation 1. By using this method, no external accuracy error is introduced into the system as the output voltage only depends on the internal reference of the TPS7H4104, which is specified across voltage, temperature and TID to be within ±1%.



$$V_{OUTx} = V_{REF} \cdot \left(1 - \frac{R_{T1} \cdot R_{T2}}{R_{B1} \cdot R_{B2}}\right) (1)$$

Fig. 6 System Level Configuration for $V_{OUTx} < V_{REF}$