

By Wibawa Chou, Eric Faraci, Srinivasan Kannan, Todd Thorp, Kelley Krch, Josemari Mapa  
IR HiRel, an Infineon Technologies Company

## Introduction

Power GaN HEMT is a promising technology for power conversion, since its material properties allow it to be a “better” switch compared to traditional Si based transistors. GaN HEMT present effective immunity to total ionizing dose (TID) and destructive single event effects (SEE) for devices with rating of around 100 V or lower, which makes them attractive for space applications.

A top challenge with space grade designs is that the highest levels of reliability is often required. Space grade component standards, like MIL-PRF-19500 JANS for discrete semiconductor devices, are based on traditional technology, such as Si, and do not include GaN. Infineon participated in recent work by a joint SAE/JEDEC working group proposing modifications to MIL-PRF-19500 to include power GaN HEMT [1-2].

## Device details

This work summarizes qualification tests and results from the first rad hard power GaN device from IR HiRel, an Infineon Technologies Company, to the proposed MIL-PRF-19500 JANS specification for power GaN HEMT.

Parameter	Value
Part number	IG1NT052N10R
Mil part number	JANSG2N7697UFHC*
Slash sheet	/794*
V <sub>DS</sub> rating	100 V
R <sub>DS(on)</sub> (typ)	3.9 mΩ
Q <sub>G</sub> (typ)	8.8 nC
Package	PowIR-SMD
TID rating	500 krad(Si)
SEE rating	GaN: 70.6 MeV·cm <sup>2</sup> /mg Si: 86.5 MeV·cm <sup>2</sup> /mg



\* MIL-PRF-19500/794 JANS qualification pending [3]

## Changes for power GaN HEMT

The following tables list key changes made to JANS screening and quality conformance inspection (QCI) tests for power GaN HEMT. The full list of screening and QCI tests for this device are in MIL-PRF-19500/794 [3].

### Screening

Test	Method	Description	Reasoning
RTGB	MIL-STD-750 1042 Con. B	25°C ±10°C, V <sub>GS</sub> =7V Shall be performed before screen 9 (interim electrical parameters)	Add an optional RTGB burn in to reduce extrinsic failures rate per Infineon GaN reliability studies
Dynamic R <sub>DS(on)</sub>	JEP173	Double pulse, see 4.5.2	Add so screening captures dR <sub>DS(on)</sub> , which does not occur in Si FET

### Group A Inspection: Electrical Verification

Subgroup	Test	Method	Description	Reasoning
A2	Dynamic R <sub>DS(on)</sub>	JEP173	Double pulse, see 4.5.2	Add dR <sub>DS(on)</sub> testing to typical DC (static) test at +25°C so screening includes dR <sub>DS(on)</sub> , which does not occur in Si FET

### Group C Inspection: Long-Term Reliability Verification, Periodic

Subgroup	Test	Method	Description	Reasoning
C2 and C6	Die shear / die pull	MIL-STD-750 2017	6 devices. May be eliminated when sufficient data is collected and approved by qualifying activity	Added to verify proper assembly of hermetic flip chip PowIR-SMD package

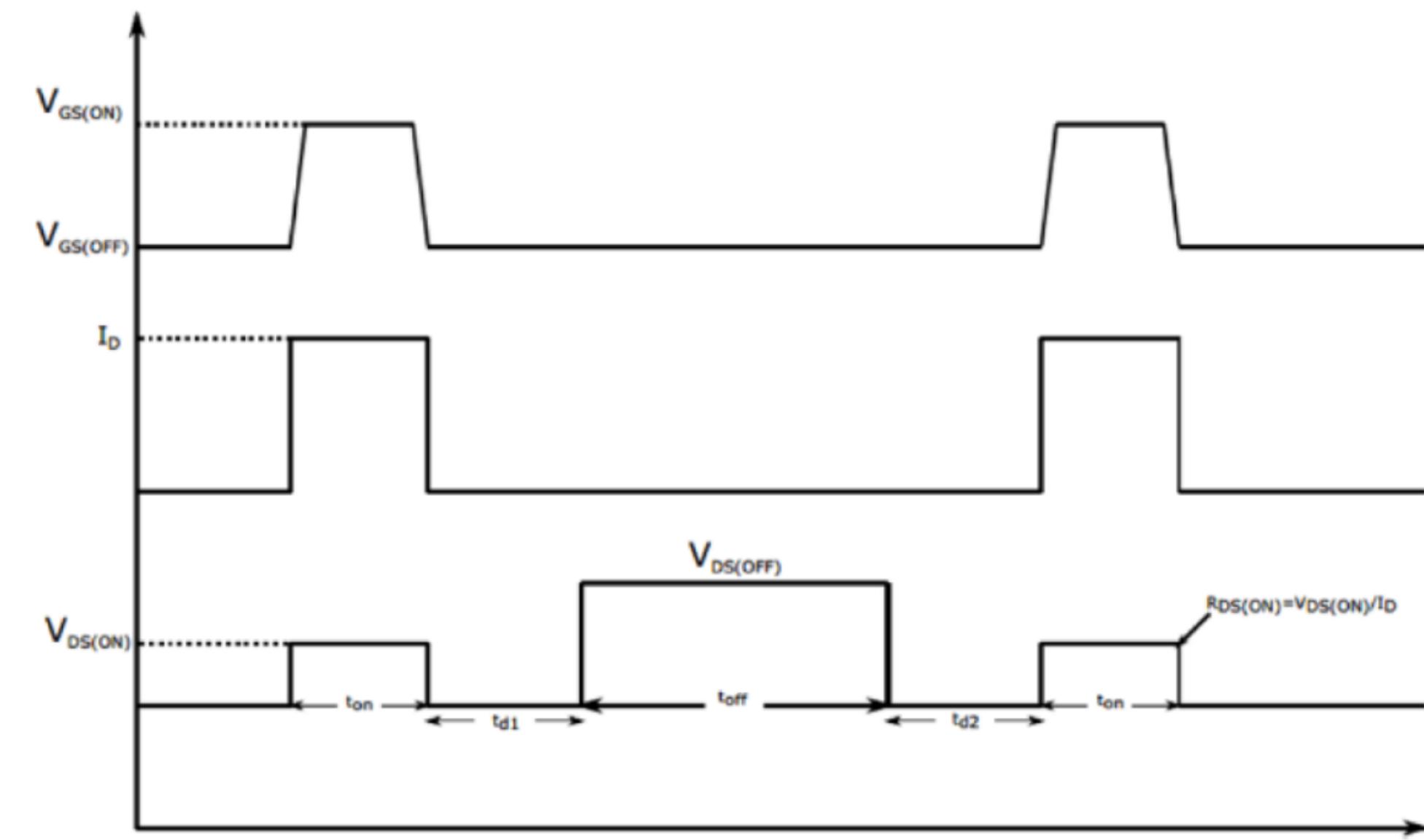
### Group E Inspection: Product Qualification

Subgroup	Test	Method	Description	Reasoning
E2	V <sub>DS</sub> transient	JEP186	Single transient at 185% rated V <sub>DS</sub> voltage for <10 µs. T <sub>J</sub> =150°C. This test may be performed at any time prior to lot formation.	Added V <sub>DS</sub> transient test before standard life tests in E2 since GaN HEMT does not have avalanche
E10	Switching dynamic life test	JEP180	Test conditions shall be derived by the manufacturer. See 4.5.4.	Added so qualification tests include hard switching and lifetime effects of dR <sub>DS(on)</sub> at conditions close to flight-like-configuration
E12	Surface mount device package integrity	MIL-STD-750 2039	Twist bend temp cycle visual, Condition C, F, T (4 devices each condition)	Added for initial package qualification of hermetic flip chip PowIR-SMD package

## Dynamic R<sub>DS(on)</sub> test details

### 4.5.2

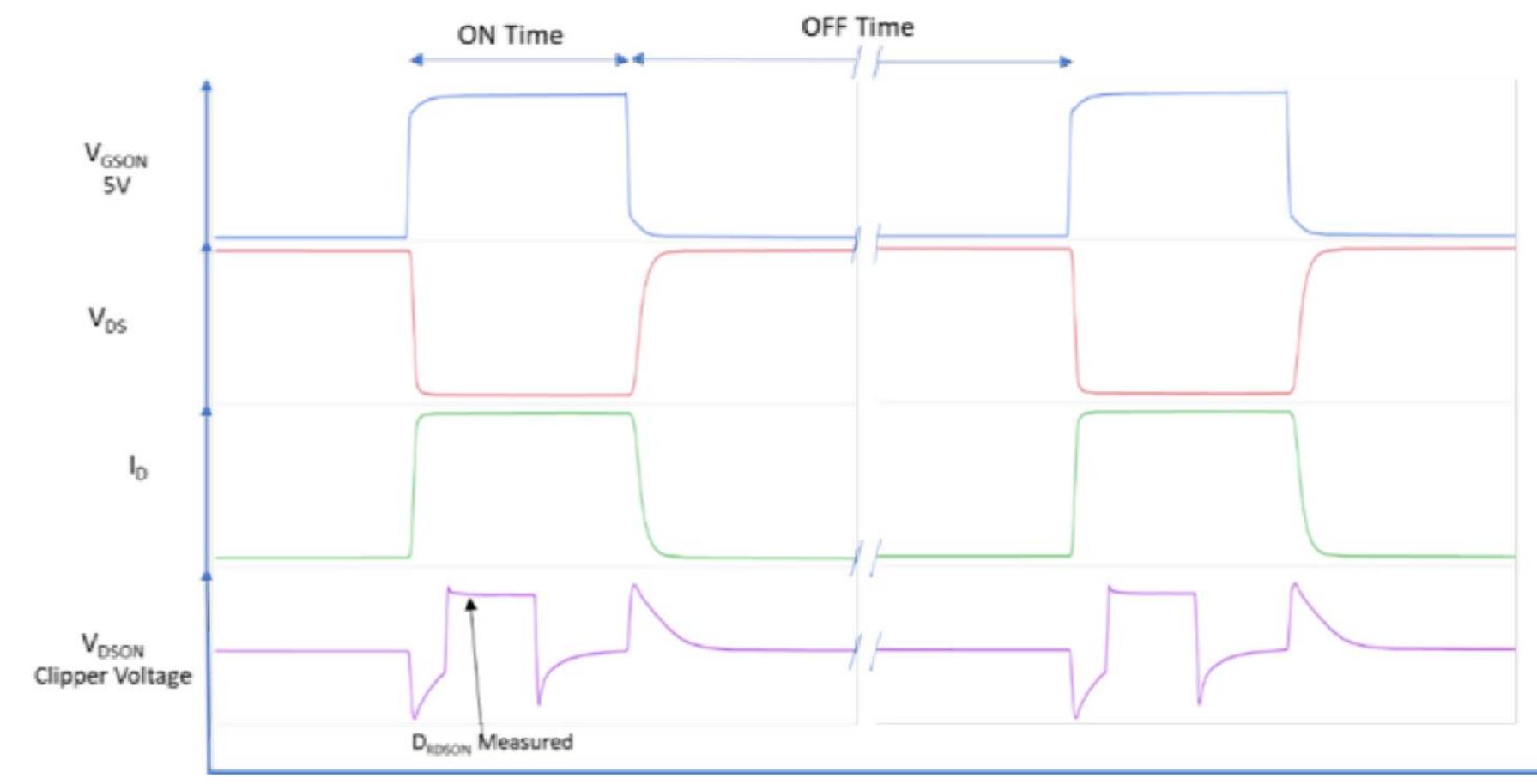
Dynamic R<sub>DS(on)</sub>: the dR<sub>DS(on)</sub> test is performed according to the pulse current voltage method of JEP173. V<sub>GS</sub>=5.0V, V<sub>DS</sub> stress = 100% rated. Stress time=5s, t<sub>on</sub> is determined by tester configuration and should be short enough to not heat the device. t<sub>d2</sub> should be less than 10µs or as fast as possible to avoid trap annealing.



### 4.5.4

Switching dynamic R<sub>DS(on)</sub>: the switching dynamic R<sub>DS(on)</sub> is performed within the guidelines of JEP180 in a hard switch test vehicle. The circuit switches a resistive load and monitors R<sub>DS(on)</sub> during the on time based on the following criteria

- V<sub>DS</sub>=45% of rated voltage
- I<sub>D</sub>=40%-60% of rated current set by resistive load to properly measure the on-state voltage drop
- T<sub>J</sub>=75°C ±10°C
- Duty cycle = 50%
- Frequency ≥ 200 kHz



## References

- R. de Leon, “Joint SAE/JEDEC GaN Power Device Working Group,” Presented at Electronics Technology Workshop (ETW), Greenbelt, Maryland, USA, June 5, 2024 [Online]. Available: <https://nepp.nasa.gov/docs/etw/2024/2024-06-05-Wed/1110-deLeon-JEDEC-GaN-Power-Device-Working-Group.pdf>
- R. de Leon, “Joint SAE/JEDEC GaN and SiC Working Group,” Presented at Components for Military & Space Electronics Conference & Exhibition (CMSE), Los Angeles, California, USA, April 30, 2024 [Online]. Available: <https://tigreenlc.com/wp-content/uploads/cmse/2024/presentations/Session%201B/1%20CMSE-2024-Presentation-deLeon-Boeing.pdf>
- Performance Specification Sheet MIL-PRF-19500/794, Defense Logistics Agency, Columbus, Ohio, March 6, 2025 [Online]. Available: <https://landandmaritimeapps.dla.mil/Downloads/MilSpec/Docs/MIL-PRF-19500/1dprf19500ss794.pdf>

