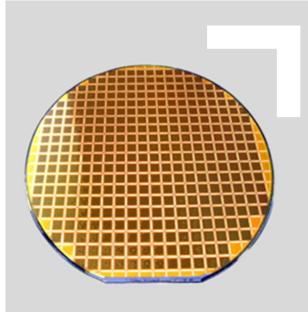
Active, All-Cell Reconfigurable Strings for Long, High Efficiency Missions

Reconfigurable Photovoltaic (PV) Arrays



P. Matthews Northrop Grumman

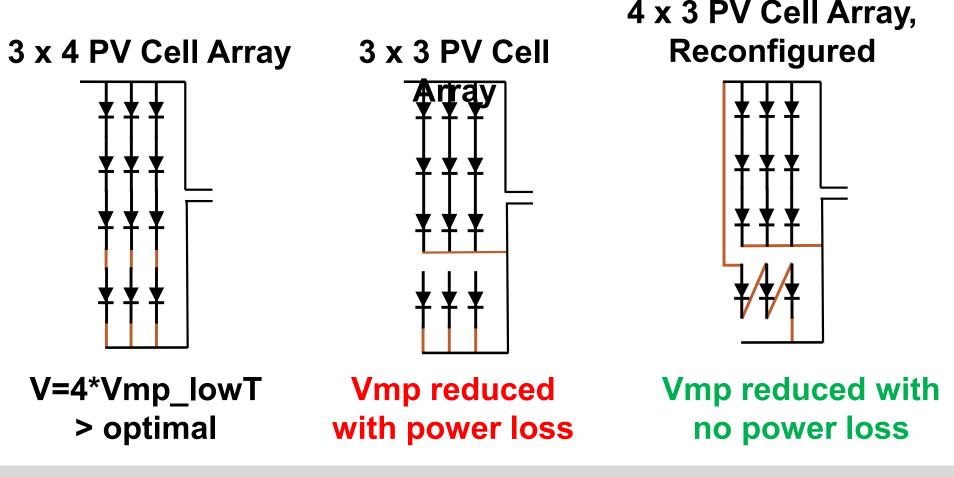
T.J. Knight Northrop Grumman

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April 23, 2024

Concept & Motivation

Mitigate Voltage Variation By PV Array Reconfiguration



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Reconfigurable strings: n x (n+1)

All Cells Are Used In All Cases

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Maintain Full PV Array Electrical Output With Reduced ΔV

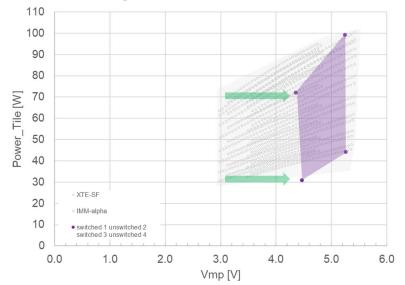
100 90 80 Power_Tile [W] 70 60 Static conventional 50 case 40 30 20 • XTE-SF 10 IMM-alpha 0 0.0 1.0 2.0 3.0 4.0 5.0 6.0 Vmp [V]

Without Switching

Simulated Temp Effects 2.8V < Vmp < 5.3V 3 x 2 Array

Reconfigurable Switching

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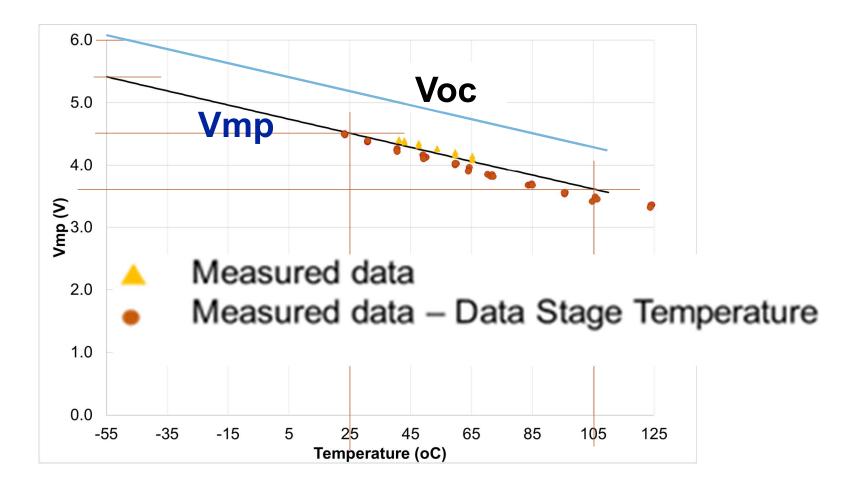
Simulated Temp Effects 4.3V < Vmp < 5.2V. $3 \times 2 \Leftrightarrow 2 \times 3$ Switching

Reduced ΔV => Greater Efficiency

110



PV Cell Modeled Vmp & Voc Plots



Voltage differential Voc – Vmp is relatively constant over temperature.

Effect of Mode Switching at 30°C 3 x 2 Array

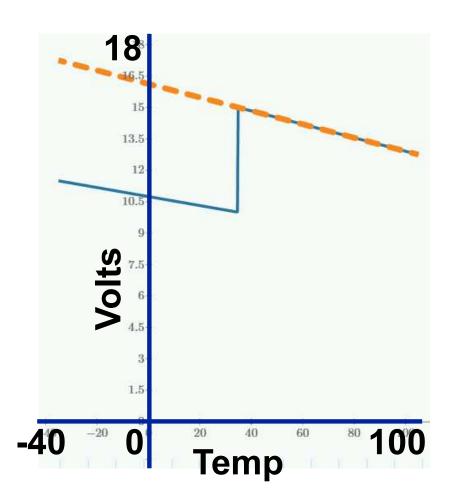


Image at left is a 2 x 3 PV cell array

Maximum Voc reduced by ~2.2V

Allows use of lower voltage switches leading to higher efficiency

This conservative analysis ignores the effect of aging, AOI, and cell type

Effect of Mode Switching at 30°C 8 x 9 Array

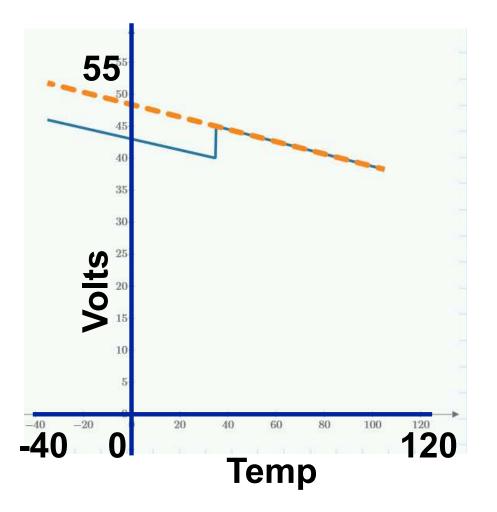
Image at right is an 8 x 9 PV cell array

Illustrates that there is an optimum ΔV configuration

A function of PV cell type, temperature, load, and the environment

This is a conservative analysis

ΔV ÷ 2





Reasons to Implement Reconfigurable Switching

- Maximize power output at all temperatures
- Limit maximum voltage
 - Allow use of lower rated converter devices with lower Rds (on)
 - Improves converter efficiency
- Limit minimum voltage
 - Allows more flexibility in component choice
 - Prevents brownout issues
- Improve overall system efficiency by reducing PV array voltage variation
 - LLC converters prefer a limited Δvin, for example
- Compensate for PV cell aging and radiation effects

Realization of Mode Switching



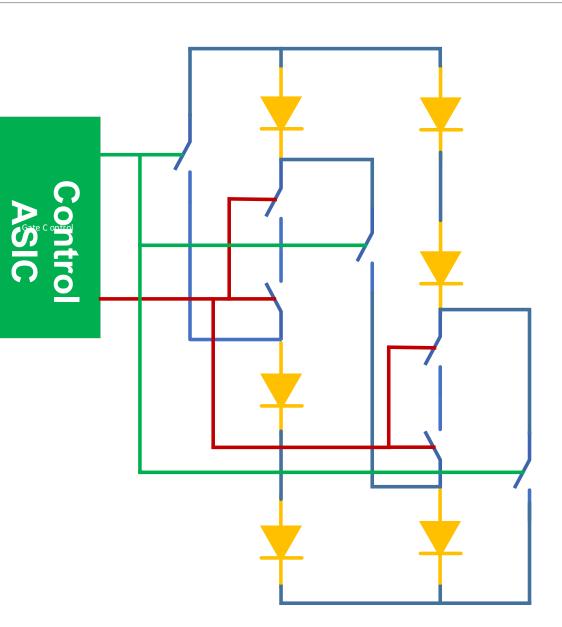
Switching Network Implementation Goals

- Minimize number of switches
 - Reduce cost and footprint
 - Maximization of PV cell packing factor reduces open area available for circuitry
- Use all N-channel switches
 - For maximum efficiency
- Implement control circuit in ASIC to minimize footprint
- Use inherently rad-hard components
- Accommodate reverse current protection
 - Control switches to prevent reverse current
 - Or, add a separate ideal diode circuit

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Reconfigurable Circuit Implementation 3 x 2

- Red 3 x Vcell
- Green 2 x Vcell
- Switches are N-channel GaNFETs
- Yellow diodes represent PV cells
- < 1mA gate drive needed
- Bootstrap supply needed for gate drive



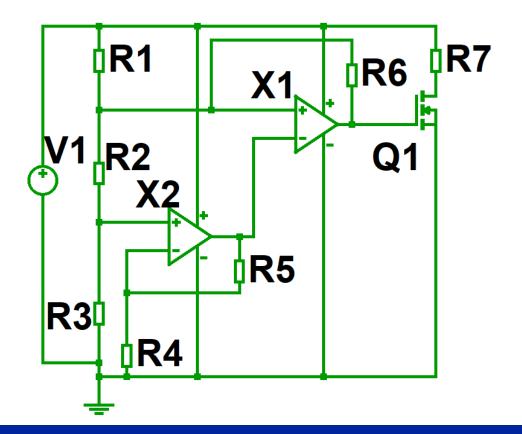


Autonomous Temperature Switch



Autonomous Local Electronic Temperature Switch

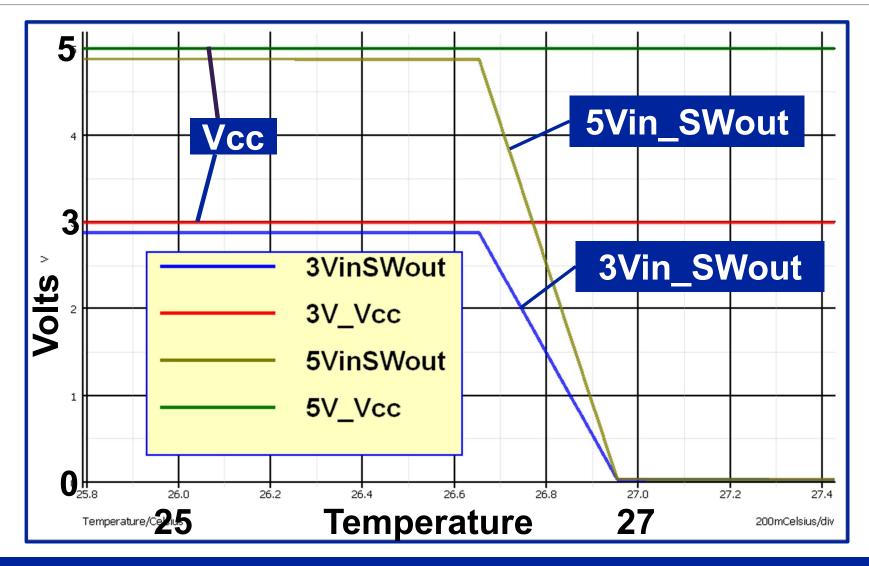
- R3 is a PTC temperature sensor, can be < 100 ohms
- No voltage reference or current source needed
- Switching temperature independent of V1 voltage
- V1 can be from PV cells
- Minimal footprint



Substantial Wiring Reduction Compared to Array-Level Control



Temperature Switch Simulation Plots



Mode Switch Temp is independent of Vcc

Summary

- A method of stabilizing a PV array output voltage while producing 100% of available power has been realized
 - Reduced ΔV increases downstream efficiency
 - Can bound array output voltage without power loss
- Readily extensible to n x (n+1) array sizes
- Minimal footprint maximizes packing factor
- Designed with radiation hardness as a requirement
- A minimal footprint autonomous temperature switch reduces wiring complexity
- Can be implemented with all N-channel devices

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