RENESAS POWER MANAGEMENT SOLUTIONS TO ADDRESS MULTI-MISSION REQUIREMENTS

APRIL 2024

ABIGAIL EBERTS
INTERSIL SPACE & HI-REL PRODUCTS
RENESAS ELECTRONICS AMERICA INC.

SUPPORTING THE BROAD SPECTRUM OF SPACE

intersil™

Increased

$ Cost

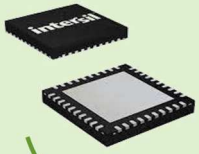
Decreased

RT Plastic
Rad Tolerant Space Plastic

Nominal LEO & MEO
Level 3 Missions

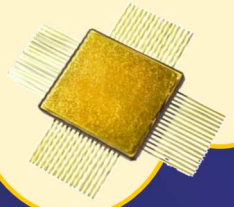
RH Plastic
QML-P; QML-P Equivalent

GEO, HEO, MEO
Level 1 & 2 Missions



RH Hermetic
QML-V and QML-V Equivalent

GEO, HEO, MEO & Deep Space
Level 1 Missions



Solution Flexibility

- Semiconductor Solution
- Rad Hard Testing
- Reliability Testing
- Package Robustness
- Package Savings

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Rad Hard Capability

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Shorter Mission Length & Nominal Requirements

Mission Life & Profile Requirements

Longer Mission Length & More Rigorous Requirements

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RAD HARD & RAD TOLERANT TEST FLOW OVERVIEW

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TEST FLOW & QUALIFICATION OPTIONS for ENVIRONMENT & APPLICATION

RH Hermetic *QML-V and QML-V Equivalent*	RH Plastic *QML-P; QML-P Equivalent*	RT Plastic *Rad Tolerant Space Plastic*
Target Orbit: MEO & GEO & HEO	Target Orbit: MEO & GEO & HEO	Target Orbit: LEO
• Highest Reliability • Most Robust Packaging Materials • Most Rigorous Test & Screen	• Very High Reliability • Packaging Materials Cost Savings • Very Rigorous Test & Screen	• Rad Tolerant Space Qualified • Packaging Materials Cost Savings • Large savings on Test & Screen
Est Mission Life >15 yrs	Est Mission Life >15 yrs	Est Mission Life <5 yrs
RLAT TID = 75-300krad(Si)	RLAT TID = 75-300krad(Si)	RLAT TID = 30krad(Si) / 50krad(Si)
SEE = LET 86 (MeV*cm^2/mg)	SEE = LET 86 (MeV*cm^2/mg)	SEE = LET 43 (MeV*cm^2/mg)
100% Burn-In & Reverse Bias Burn-In w/Deltas & PDA Calculation w/Pre-Mid-Post Burn-In Elec Test	100% Burn-In & Reverse Bias Burn-In w/Deltas & PDA Calculation w/Pre-Mid-Post Burn-In Elec Test	Not Performed Not Offered Not Performed
Tri-Temp Test: -55°C, 25°C, 125°C	Tri-Temp Test: -55°C, 25°C, 125°C	Room Temp 25°C Test Only
Serialized Units w Data Packet	Serialized Units w Data Packet	TID Data Packet

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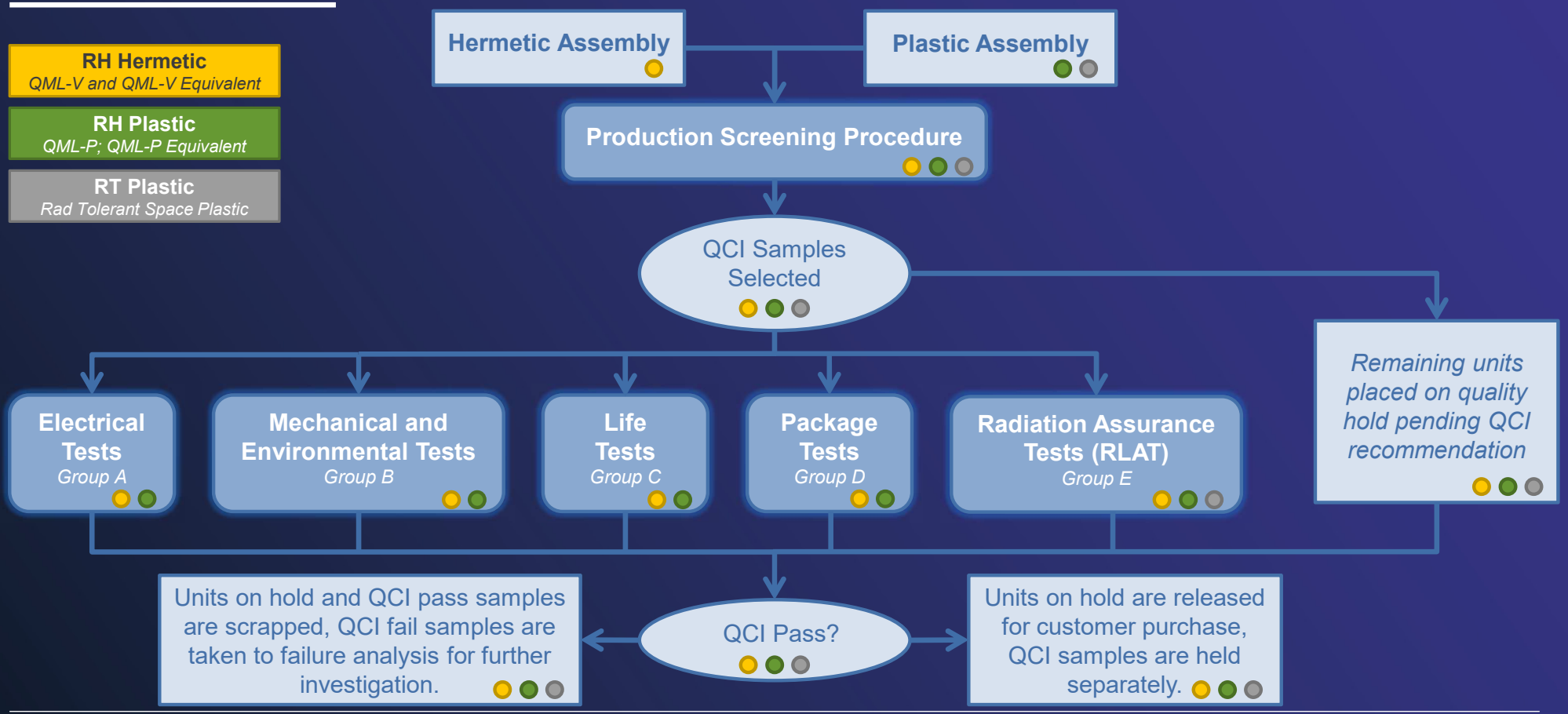
PRODUCTION FLOW



PRODUCTION FLOW COMPARISON (100%)

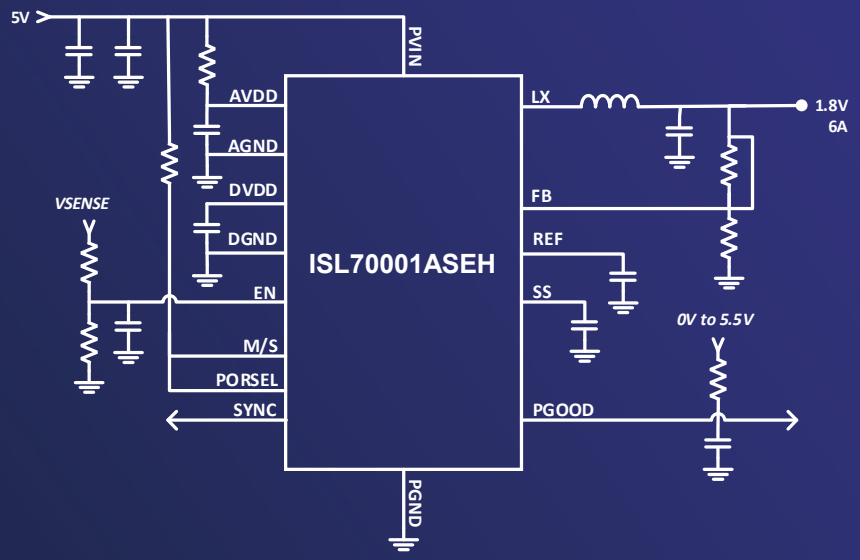
	RH Hermetic	RH Plastic	RT Plastic
Wafer Lot Acceptance	✓	✓	✓
Non-destructive Bond Pull	✓	*Unnecessary for plastic package*	
Internal Visual Inspection	✓	✓	
Temperature Cycling	✓	*Unnecessary for plastic package*	
Constant Acceleration	✓	*Unnecessary for plastic package*	
Visual Inspection	✓	✓	
Particle Impact Noise Detection (PIND) Test	✓	*Unnecessary for plastic package*	
Fine/Gross Leak	✓	*Unnecessary for plastic package*	
Serialization	✓	✓	
X-Ray	✓	✓	
Pre/Post Burn-In Electrical Test	✓	✓	

	RH Hermetic	RH Plastic	RT Plastic
Burn-In Test	✓	✓	
Reverse Bias (Static) Burn-In Test	✓	✓	
Percent Defective Allowable Calculation	✓	✓	
Final Electrical Test (-55°C, +25°C, +125°C)	✓	✓	✓ *+25°C only*
Acoustic Microscopy	*Unnecessary for hermetic package*	✓	
External Visual Inspection	✓	✓	✓
QCI Group A	✓	✓	
QCI Group B	✓	✓	
QCI Group C	✓	✓	
QCI Group D	✓	✓	
QCI Group E (RLAT)	✓	✓	✓

INITIAL QUALIFICATION VS ONGOING SCREENING

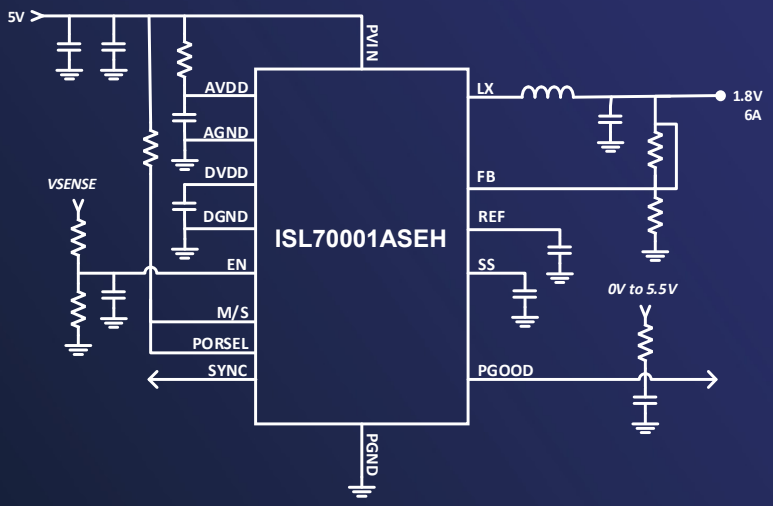
	Initial Qual	Ongoing Screen	Initial Qual	Ongoing Screen	Initial Qual	Ongoing Screen
	RH Hermetic		RH Plastic		RT Plastic	
Package-Related Tests						
Soldering Heat	✓		*Unnecessary for plastic package*		*Unnecessary for plastic package*	
Moisture Resistance Testing to Determine MSL	*Unnecessary for hermetic package*		✓		✓	
Biased/Unbiased Highly Accelerated Stress Test (HAST)	*Unnecessary for hermetic package*		✓	✓	✓	
High Temperature Storage	*Unnecessary for hermetic package*		✓		✓	
Temperature Cycle		✓	✓	✓	✓	
Device-Related Tests						
ESD	✓		✓		✓	
Latch-Up	✓		✓		✓	
High Temperature Operational Life (HTOL)		✓	✓	✓	✓	
Radiation Related Tests						
TID: HDR and/or LDR (RLAT), per datasheet spec	✓	✓	✓	✓	✓	✓
Destructive Single Event Effects (DSEE)	✓		✓		✓	
Single Event Transient (SET)	✓		✓		✓	

SIMPLIFY DESIGN PROCESS WITH A SINGLE SCHEMATIC



ISL70001ASEH
6A Synchronous Buck Regulator
5V input, 1.8V 6A output schematic

SIMPLIFY DESIGN PROCESS WITH A SINGLE SCHEMATIC



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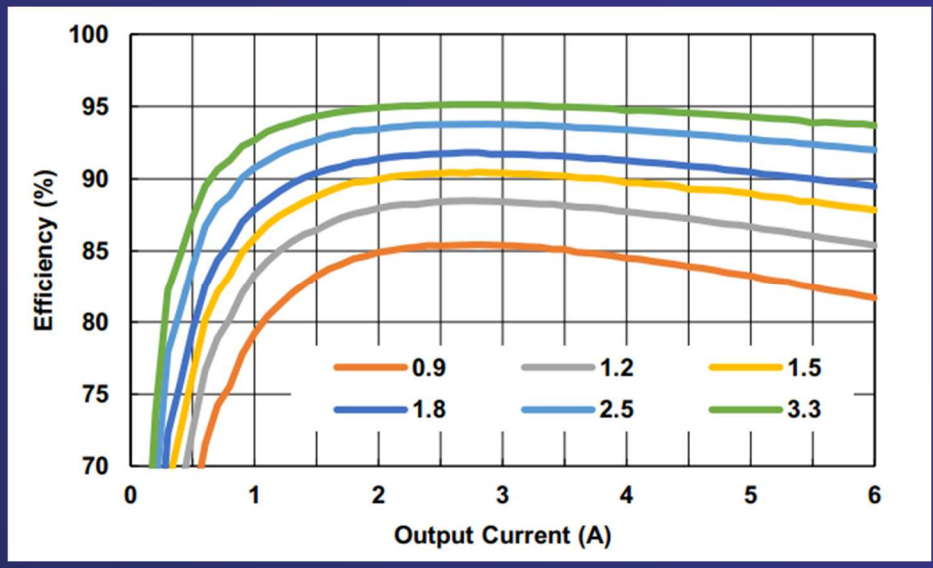
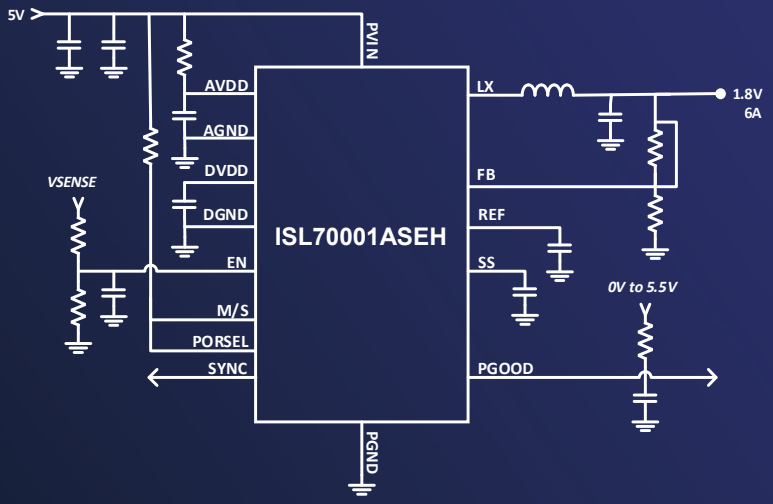


5V V_{IN} Efficiency for Multiple V_{OUT} Levels

SIMPLIFY DESIGN PROCESS WITH A SINGLE SCHEMATIC



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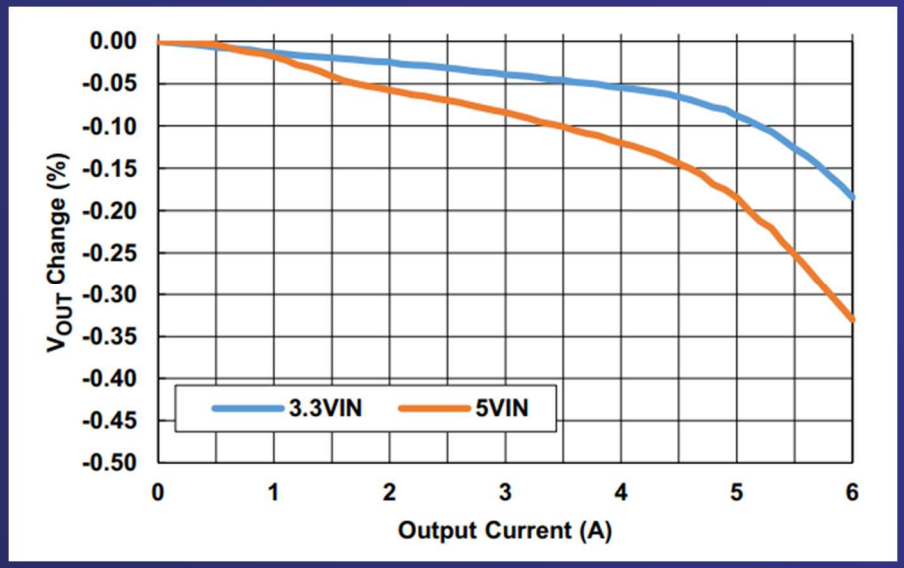
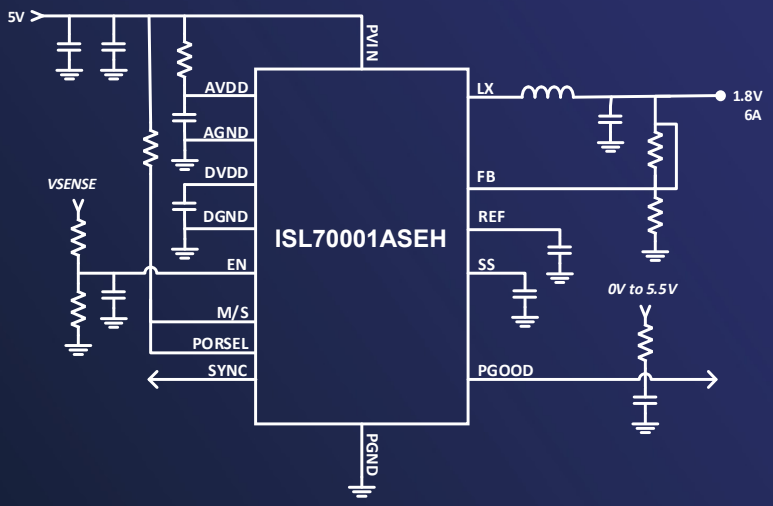


V_{IN} Load Regulation, V_{OUT} = 1.2V

SIMPLIFY DESIGN PROCESS WITH A SINGLE SCHEMATIC



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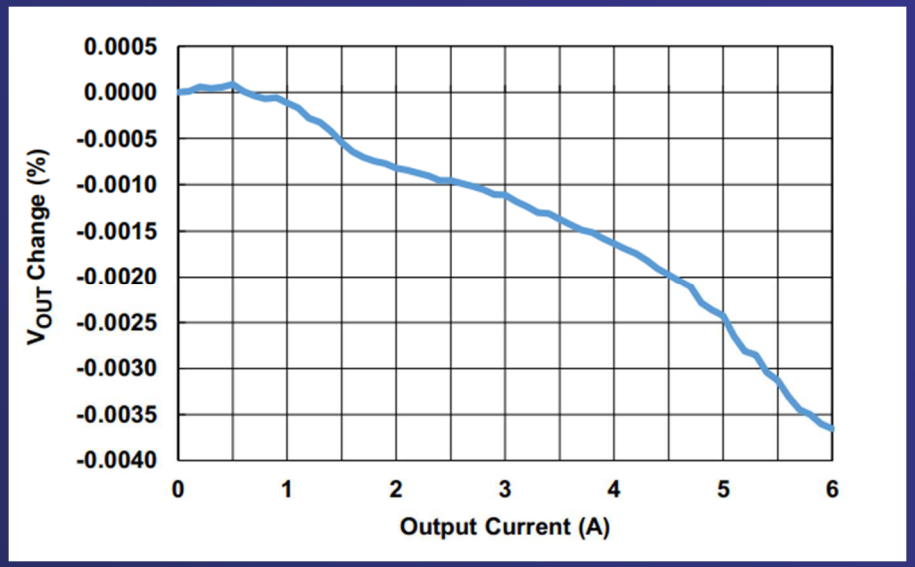
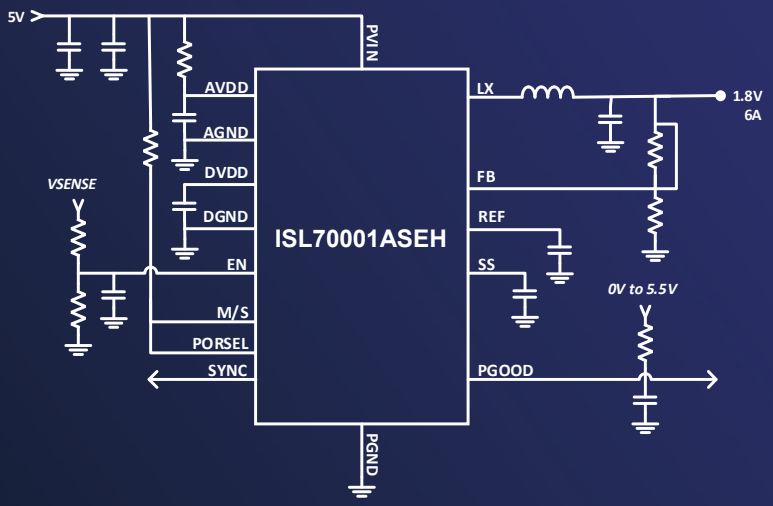


V_{IN} Line Regulation, V_{OUT} = 2.5V (5V_{IN} – 3.3V_{IN})

SIMPLIFY DESIGN PROCESS WITH A SINGLE SCHEMATIC



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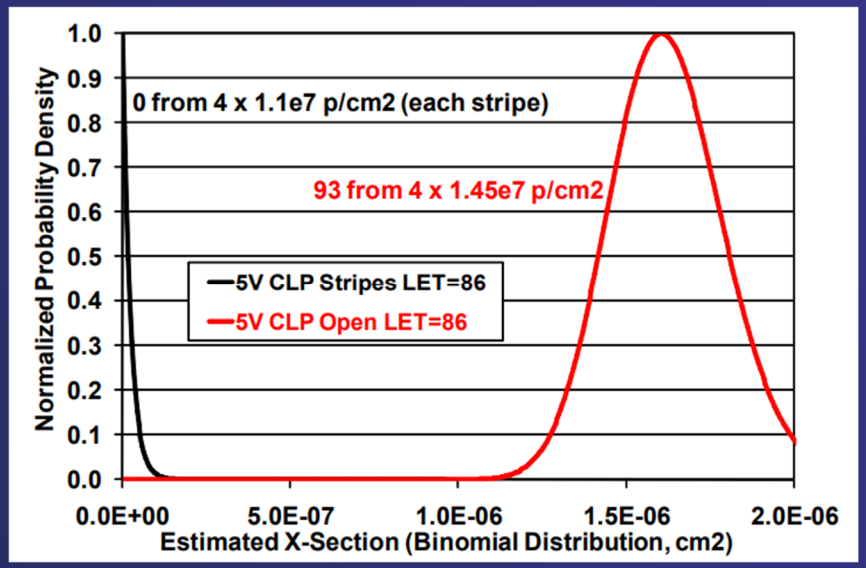
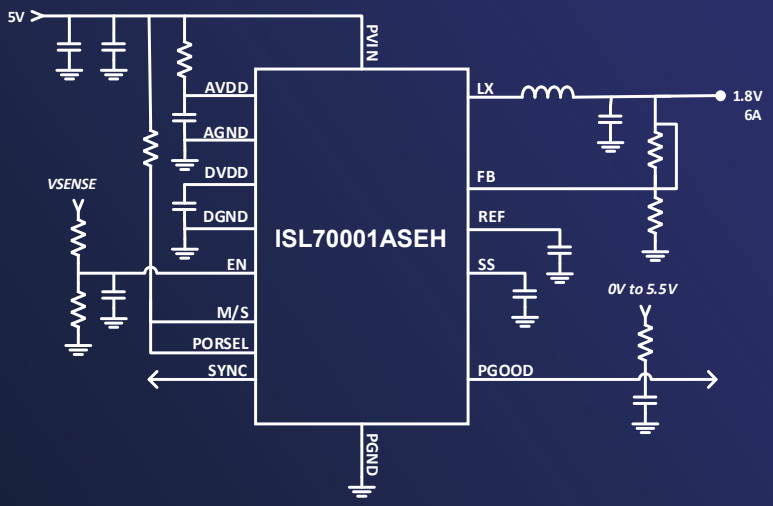


Estimated SET Cross-Sections of Shielded (Black) and Unshielded (Red) Units Assuming a Binomial Distribution
**Results offer proof that non-benign SETs are the result of high flux test rates*

SIMPLIFY DESIGN PROCESS WITH A SINGLE SCHEMATIC



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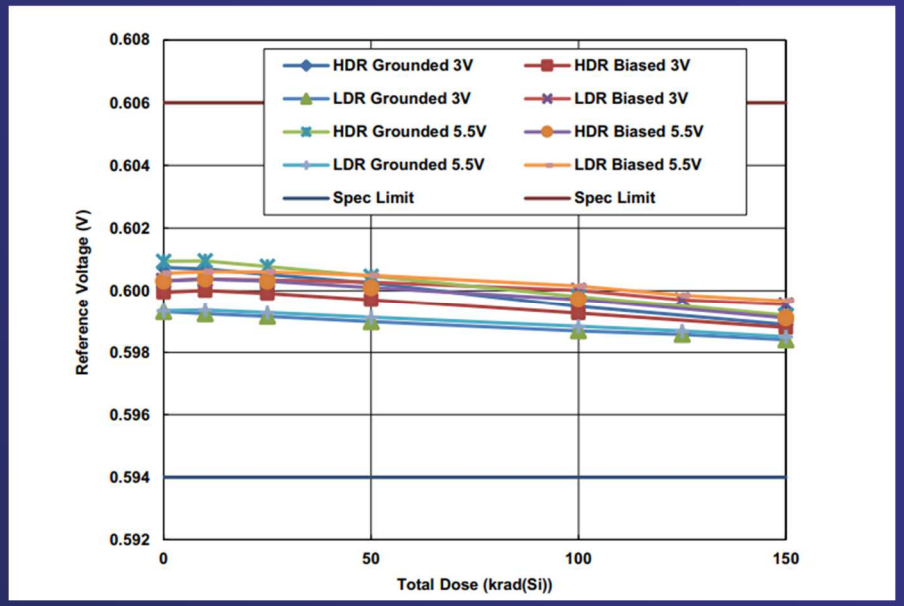
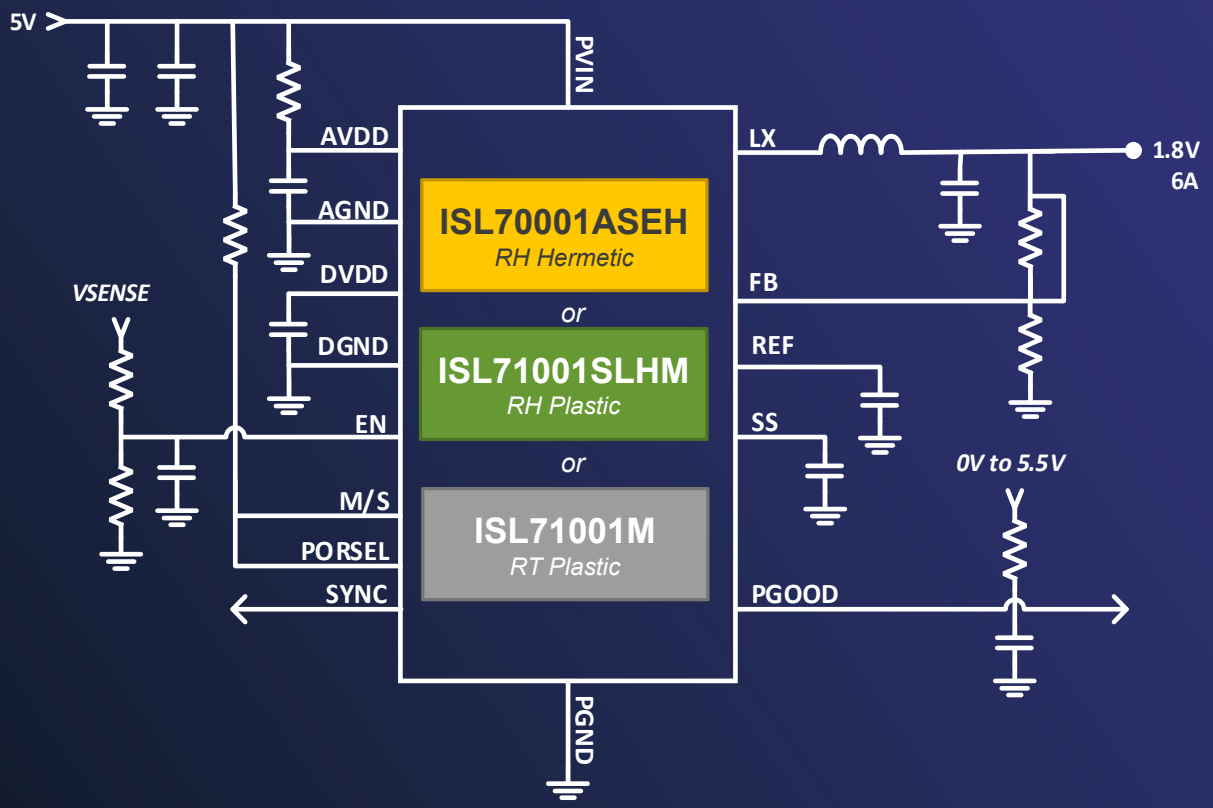
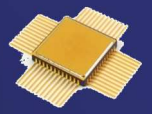


ISL70001ASEH reference voltage as a function of total dose irradiation at LDR and HDR for unbiased and biased cases

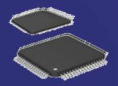
SIMPLIFY DESIGN PROCESS WITH A SINGLE SCHEMATIC



- 1 Schematic
- 3 Qualification Levels
  - Level 1 Missions: ISL70001ASEH
    RH Hermetic
  - Level 1& 2 Missions: ISL71001SLHM
    RH Plastic
  - Level 3 Missions: ISL71001M
    RT Plastic
- 2 Package Options



48 ld. CQFP w/ optional heat sink



12x12 64 ld. ep TQFP

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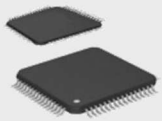
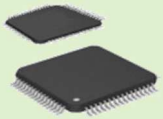
ISL71001M
RT Plastic

Nominal LEO & MEO
Level 3 Missions



ISL71001SLHM
RH Plastic

GEO, HEO, MEO
Level 1 & 2 Missions



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GEO, HEO, MEO
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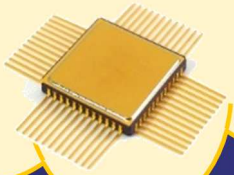

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- Reliability Testing
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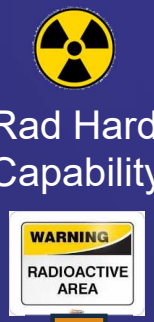
Rad Hard Capability



Decreased

Shorter Mission Length & Nominal Requirements

Mission Life & Profile Requirements

Longer Mission Length & More Rigorous Requirements

RENESAS

QUESTIONS?

Abigail Eberts

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Applications Engineer

Intersil Space/Hi-Rel Products