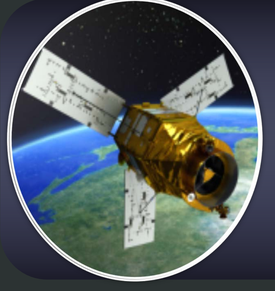

Design of Precharge Circuit with Latched Current Limiter for Power Control and Distribution Unit in Low Earth Orbit Satellite

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I. INTRODUCTION

Power control and distribution unit is essential component in low earth orbit satellite systems, as it provides power to various subsystems and loads. However, the operation of the loads can be affected by various factors, such as voltage fluctuations, inrush current, and overcurrent conditions. To ensure stable operation of the loads, PCDU may implement various protection features, such as precharge circuit with a latched current limiter.

In this paper, we focus on the design and implementation of a precharge circuit with a latched current limiter for a PCDU in low earth orbit satellite system. The latched current limiter is designed to protect the loads from overcurrent conditions, while the precharge circuit is intended to limit inrush current during startup. We describe the design and implementation of these features in detail, including the selection of appropriate components and the calculation of relevant parameters.

II. DESIGN AND IMPLEMENTATION

To improve the performance of the PCDU, we implement a soft-start feature using a FET turn-on slew rate. However, adjusting the gate-source capacitor of the FET to control the FET's turn-on slew rate may not be sufficient in situations with very high inrush current. In such cases, a latched current limiter can be triggered, causing the FET to switch off, or the FET may not be able to turn on due to the latched current limiter trip-off limitations.

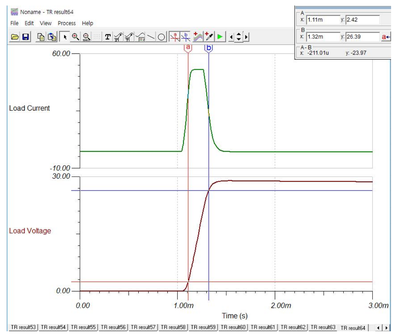
The precharge circuit is implemented using a high-power resistor, which is connected in series with the precharge line and in parallel with the main power supply line. The resistance value is selected based on the capacitance of the load and the desired precharge time. The resistance limits the inrush current during startup, preventing voltage spikes and other undesirable effects.

III. EXPERIMENTAL RESULTS

1) Simulation Result

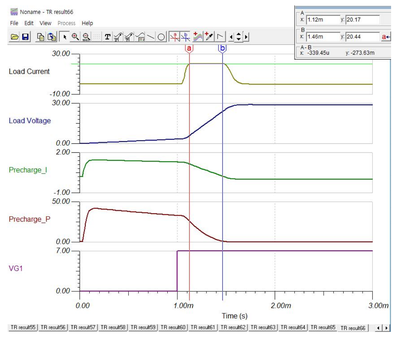
a) Inrush current characteristics

- *Simple Capacitive Load*
- *Max. Current = 50A*
- *Output Voltage Slope ≈ 200us*



b) Simulation result with precharge R=20Ω

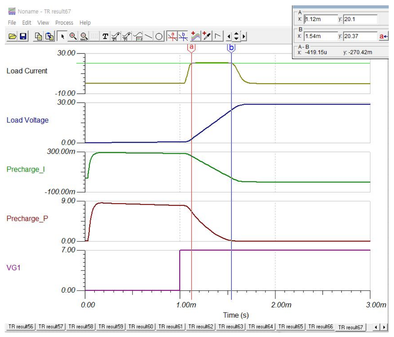
- LCL Trip-off Level = 20A
- LCL duration ≈ 340us (<400us)
- Power Consumption of Rpre > 40W



While it satisfies the 400us Trip-off duration, which is the junction temperature (Tj) limit of the FET, it is realistically impossible due to the power consumption of the precharge resistor exceeding 40W.

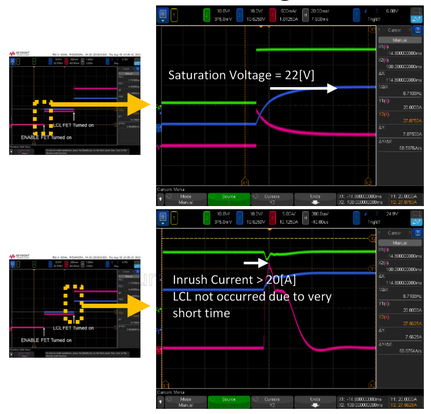
c) Simulation result with precharge R=100Ω

- LCL Trip-off Level = 20A
- LCL duration ≈ 420us (>400us)
- Power Consumption of Rpre ≈ 9W



While the power consumption of the precharge resistor complies with the 40W requirement, the trip-off duration exceeding the 400us limit, which is the junction temperature (Tj) boundary for the Field-Effect Transistor (FET), renders it realistically unfeasible.

2) Test Result with Precharge R=28.8Ω



$$E = \left(\frac{1}{3} \times I^2 \times R \times t_1\right) + \left(\left(-I^2 \times R \times \frac{\tau}{2}\right) \times \left(e^{-\frac{2\times(t_3-t_1)}{\tau}} - 1\right)\right)$$

$$= \left(\frac{1}{3} \times 20^2 \times 28.8 \times 40 \times 10^{-6}\right) + \left(\left(-20^2 \times 28.8 \times \frac{288.54}{2} \times 10^{-6}\right) \times \left(e^{-\frac{2\times(400)}{288.54}} - 1\right)\right)$$

$$= 0.154 + 1.558 = 1.712\text{Ws or J}$$

$$where,\ t_1 = 40\mu s, t_2 = 240\mu s, t_3 = 440\mu s, \tau = -\frac{t_2 - t_1}{\ln(0.5)} = 288.54\mu s$$

a) The percentage of pulse energy to pulse handling capability @ ambient temperature of 25°C

$$\frac{E}{E_R} \times 100 = \frac{1.712\ Ws}{3.75\ Ws} \times 100 = 45.65\% < 100\%\ (recommendation)$$

b) The percentage of pulse energy to pulse handling capability @ maximum temperature of 125°C

$$\frac{E}{E_R} \times 100 = \frac{1.712\ Ws}{2.25\ Ws} \times 100 = 76.09\% < 100\%\ (recommendation)$$

c) The percentage of pulse energy to pulse handling capability with paralleled R @ 125°C

$$\frac{E}{E_R} \times 100 = \frac{1.712\ Ws}{2.25\ Ws} \times \frac{1}{2} \times 100 = 38.05\% < 100\%\ (recommendation)$$

IV. CONCLUSION

- In this paper, we presented the implementation of a latched current limiter and a precharge resistance for a PSU in a satellite system. The protection features are designed to ensure stable operation of the loads under various conditions, such as overcurrent conditions, inrush current, and voltage fluctuations. The experimental results demonstrate the effectiveness of the proposed approach, and the PSU is shown to perform reliably under all tested conditions.