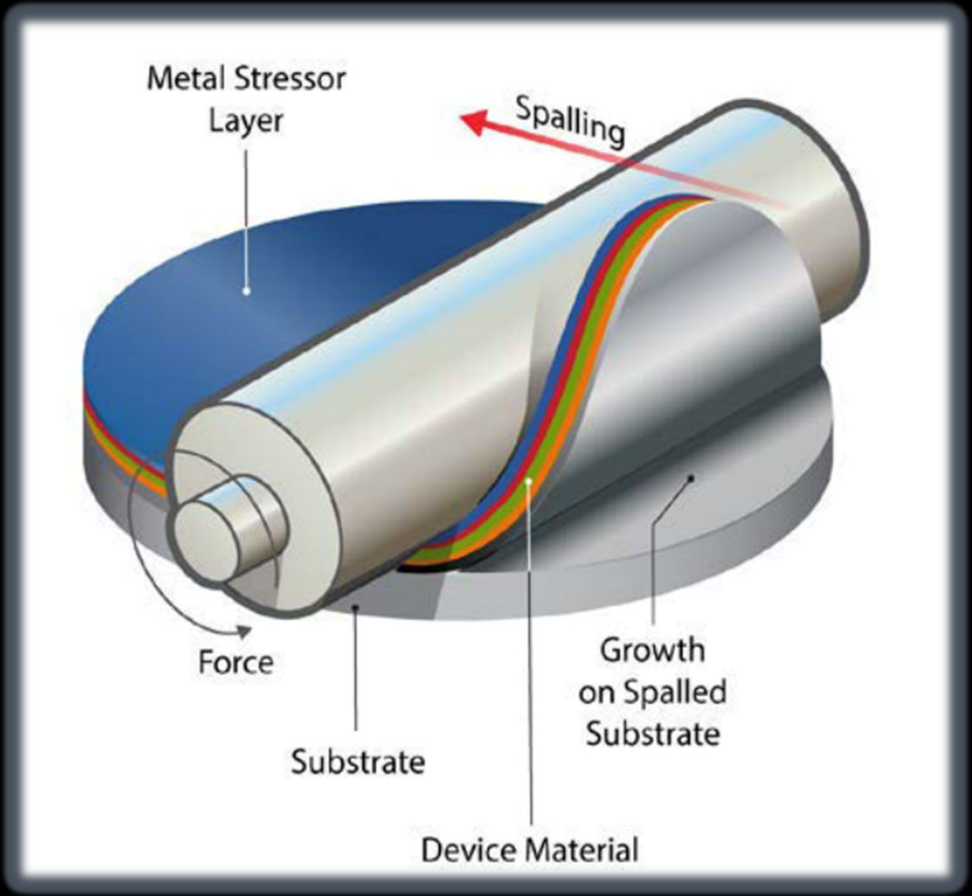
Wafer reuse via controlled spalling for lowering space photovoltaic cell cost



April 2023 Space Power Workshop

Corinne E. Packard, Aaron J. Ptak

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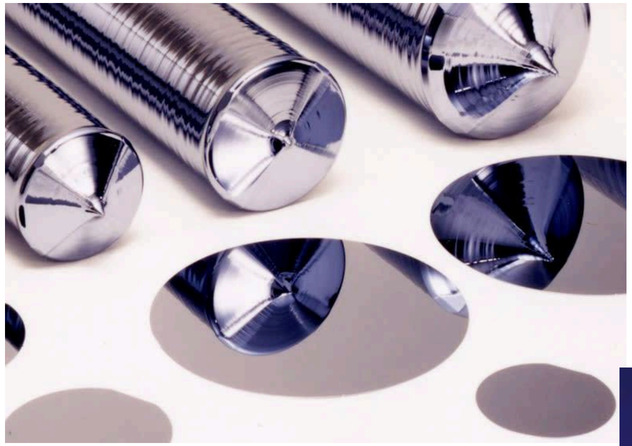
NREL Transforming ENERGY

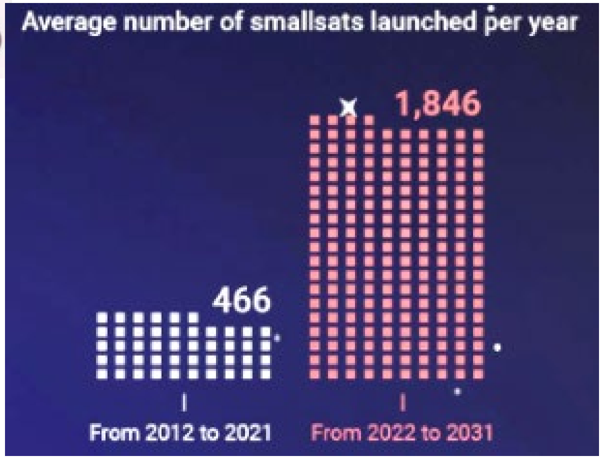
Value tied up in the PV cell substrate

Substrate costs are a major limitation to lowering the cost of high-efficiency III-V photovoltaics



Substrate: ~$36/W, about 40% of cell direct manufacturing cost

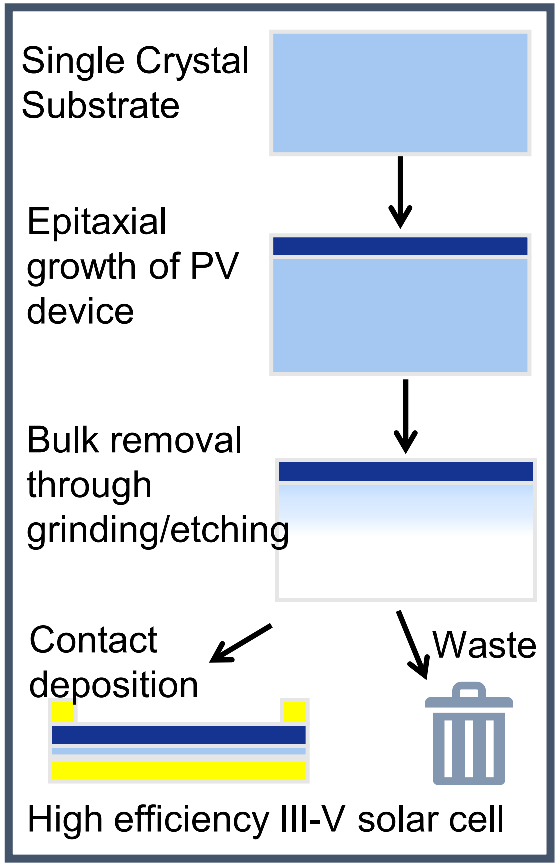
Substrate demand is expected to rise exponentially with expansion of space programs



For III-Vs, Wafer thickness ≠ Cell thickness

Active region 2-25 μm

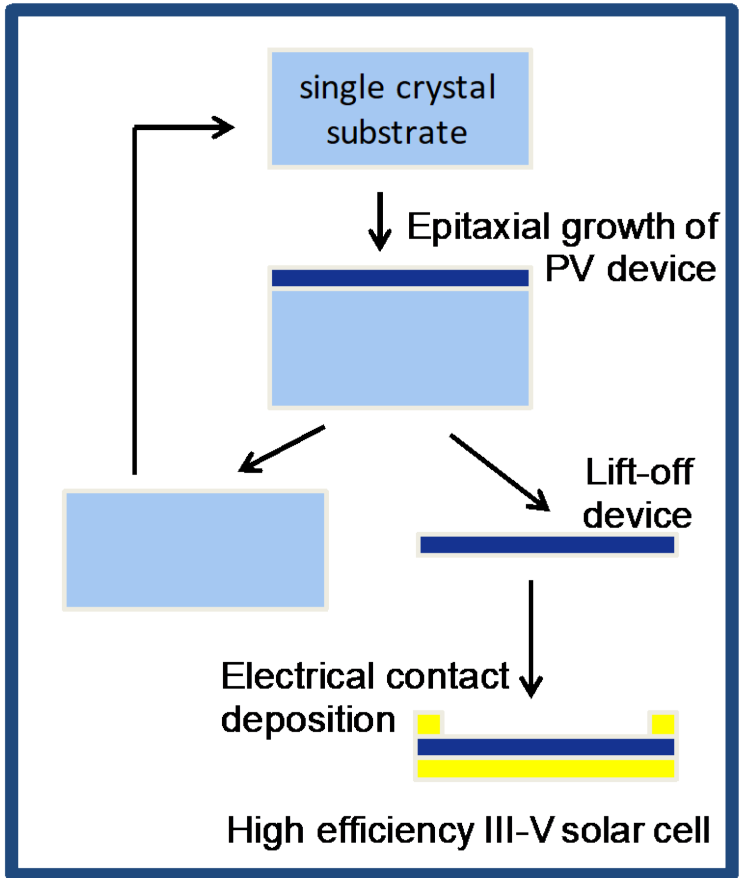
Wafer value consumed as waste



K. Horowitz, et al., NREL/TP-6A20-72103. 2018
Euroconsult "Prospects from the Small Satellite Market" 8th ed.

Opportunities to extract value from the PV cell substrate with device exfoliation and wafer reuse

Wafer Substrate Reuse



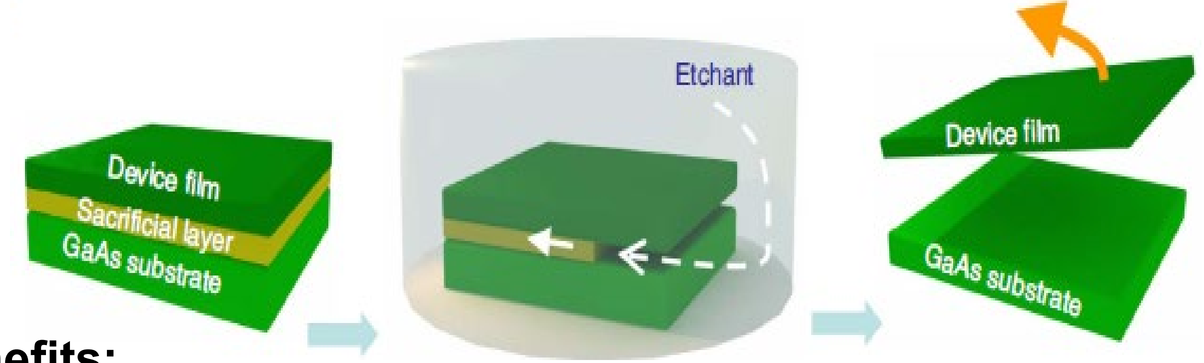
Recycle- remove device and put substrate in recycling stream as high purity scrap

Reclaim- polish to epi-ready standards before reuse of thinner substrate

Direct reuse- epi growth on substrate after device removal with minimal surface preparation

Fracture-based reuse- an alternative to ELO

Epitaxial Lift-Off (ELO) – the only commercially adopted exfoliation method
Selective chemical etch of ~10nm-thick release layer in high concentration HF acid

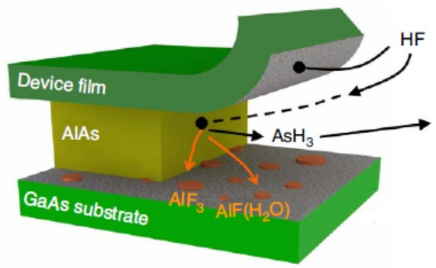


Benefits:

- Produces flat substrate and flat device surface

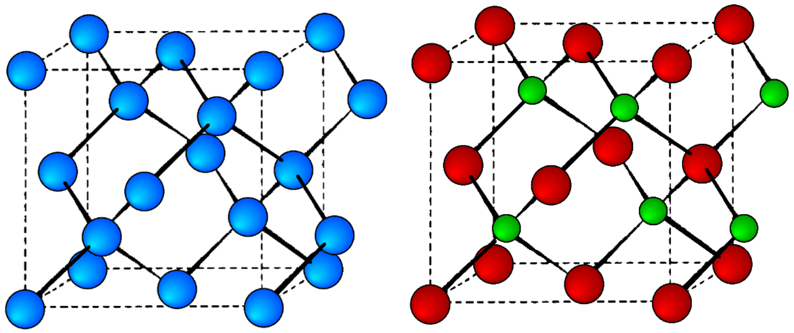
Drawbacks:

- GaAs only, no Ge (misses 80% of space PV)
- Must avoid or protect Al-containing layers
- Transport-limited: slow & scales poorly
- Pitting and accumulation of etch products impede reuse without repolishing



Potential Alternative:
Use a lateral fracture to remove device instead

- Fracture is FAST
- Fracture can be CLEAN



Fracture in the substrate opens fresh surfaces within the crystal

C.-W. Cheng, et al., Nat. Commun., 2013. 4(1): p. 1577.

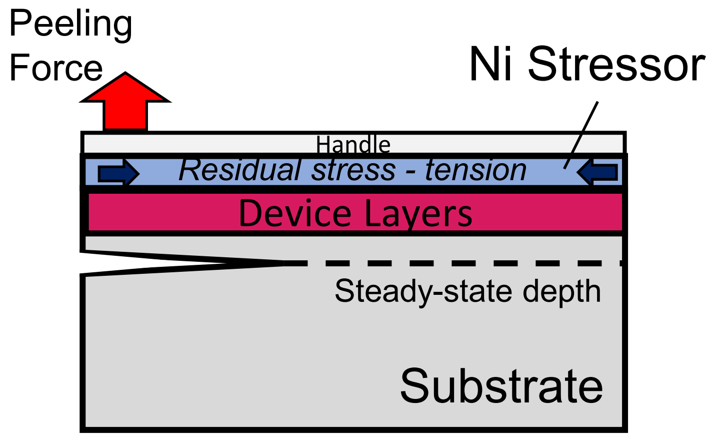
https://chem.libretexts.org

Controlled Spalling methods

Fracture-based process-

Exploits natural mechanism of spalling fracture, but the release is controlled

Requirements:
High tensile-stressed film applied to device/substrate
Strong film material → *suppresses cracking*
Good adhesion → *suppresses delamination*



First developed as an exfoliation technology for III-Vs by IBM Watson Research Center

These conditions generate a buried stress field with tensile stress concentrated at a specific depth.

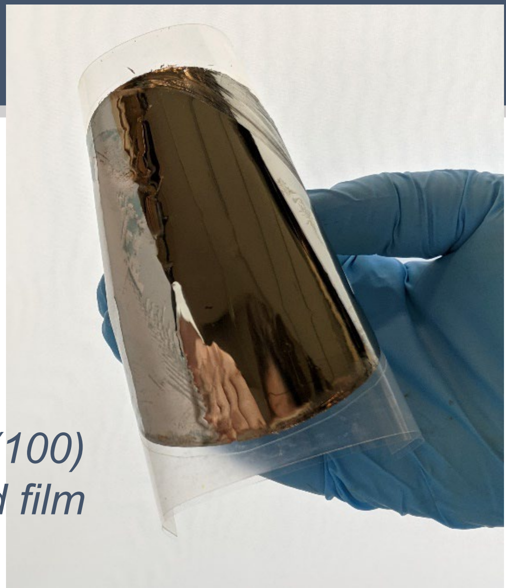
Fracture depth is targeted to be below the device layers, by tuning stress and thickness.

Fracture creates chemically pristine surfaces on device and remaining substrate

Wafer-scale controlled spalling results

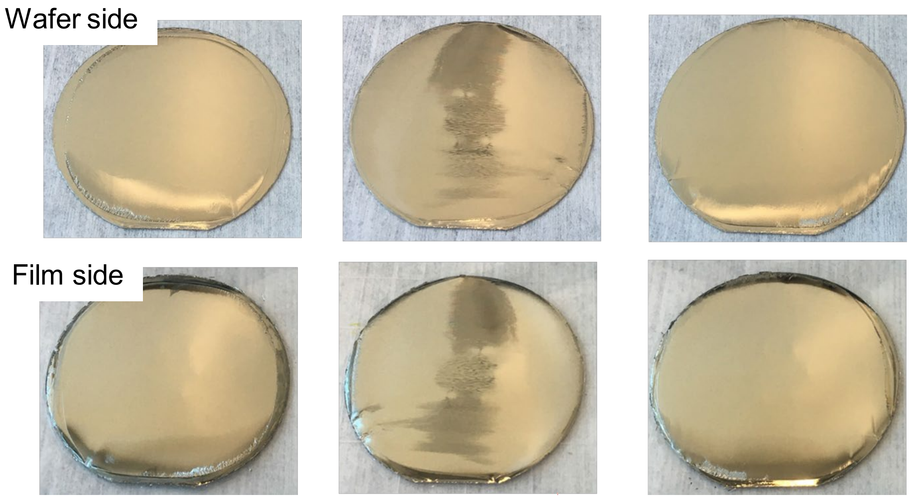
50
Ga

My reflection in the center of a spalled Ge wafer



100 mm Ge (100) spalled film

Three 50 mm Ge (100) wafers



Spalled wafers, edge-to-edge

- 50 mm & 100 mm Ge (100)
- 50 mm GaAs (100) and (110)

Spalled film thicknesses of
1-80 μm in Ge and 5-100 μm in GaAs (100)
→ Appropriate for device liftoff and kerfless wafering

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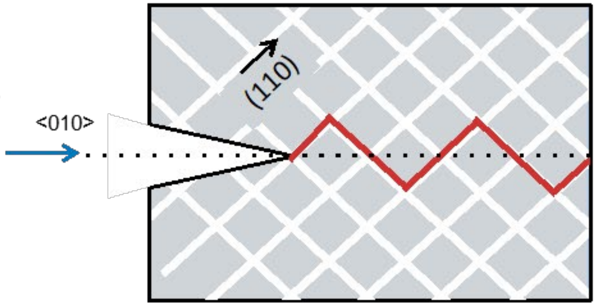
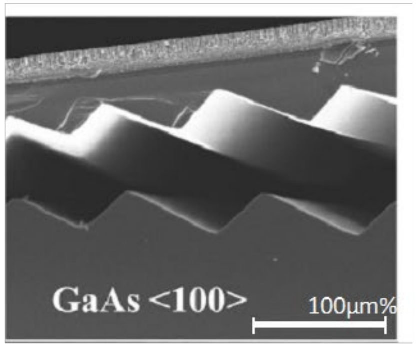
Availability of low energy fracture planes dictates surface structure
Unlike in Ge, (100) cleavage is not available for GaAs

(100)-GaAs wafer

Regular sawtooth facets



Fracture planes oriented 45° from steady-state spalling depth

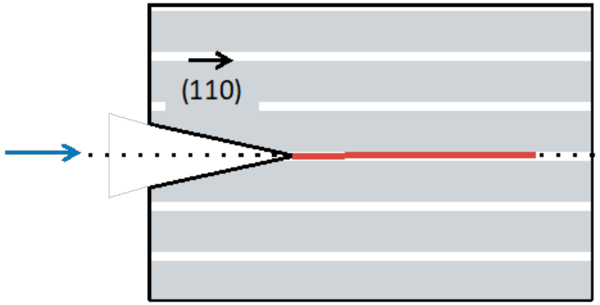


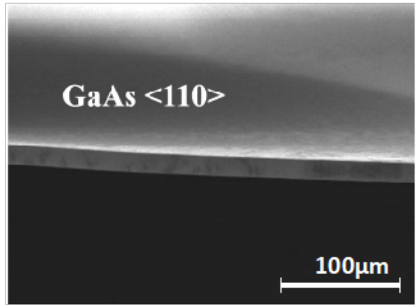
IBM, Bedell, J. Photovolt. IEEE v. 2 (2012)

SEM cross-section GaAs spalling

(110)-GaAs wafer

Smooth





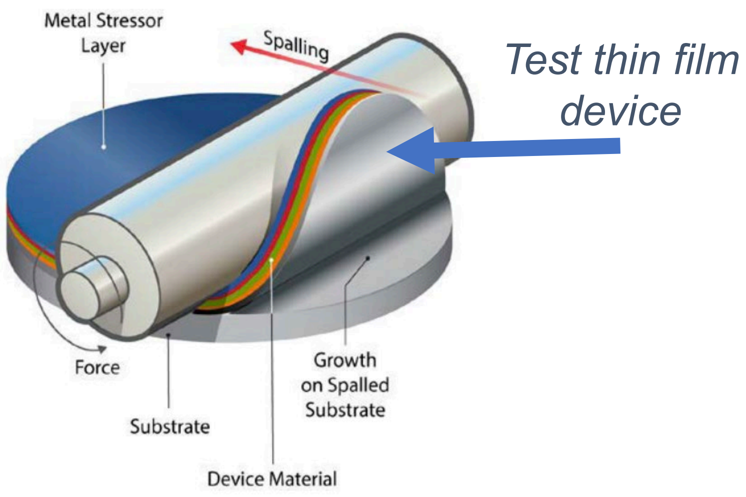
IBM, Bedell, J. Photovolt. IEEE v. 2 (2012)

Controlled spalling does not create defects that impact device performance

Device structures grown on epi-ready substrates, then spalled off and processed

Cell Type	Substrate	V_{OC} (V) **Spalled** Control	J_{SC} (mA/cm^2) **Spalled** Control	Efficiency (%) **Spalled** Control	Source
Upright 1-J Ga(In)As With ARC	Ge No orientation given	**1.011** 1.018	**22.9** 22.6	**16.9** 17.1	Bedell et al. 2012
Inverted 2-J GaInP/Ga(In)As With ARC	Ge (100)	**2.312** 2.287	**14.0** 13.9	**28.1** 26.6	Shahjerdi et al. 2013
Upright 3-J GaInP/Ga(In)As/Ge With ARC	Ge (100)	**2.488** 2.553	**13.7** 13.7	**28.7** 30.5	Shahjerdi et al. 2012
Inverted 1-J GaAs No ARC	GaAs (100)	**1.072** 1.070	**20.2** 20.4	**18.2** 18.4	Sweet et al. 2016

Devices all grown by MOCVD and tested under AM1.5 G 1 sun intensity (1000 W/m^2)



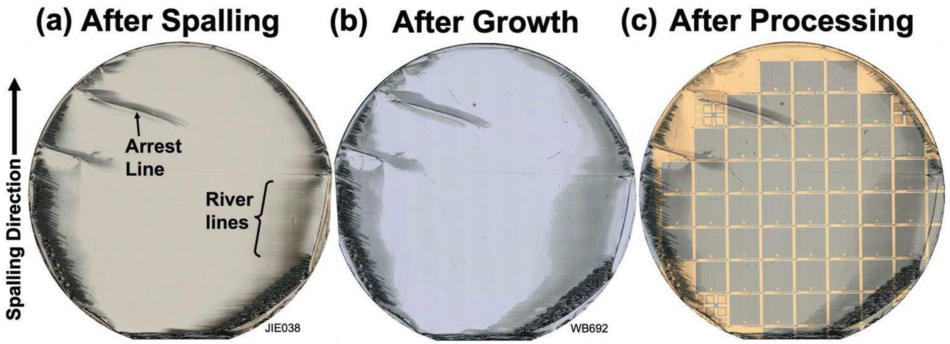
Parity performance across multiple device structures

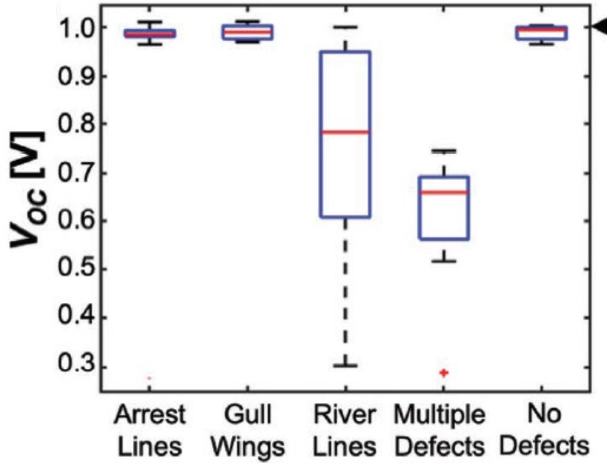
No evidence of dislocation formation in devices or substrates

Summarized in Chen & Packard SOLMAT 2021

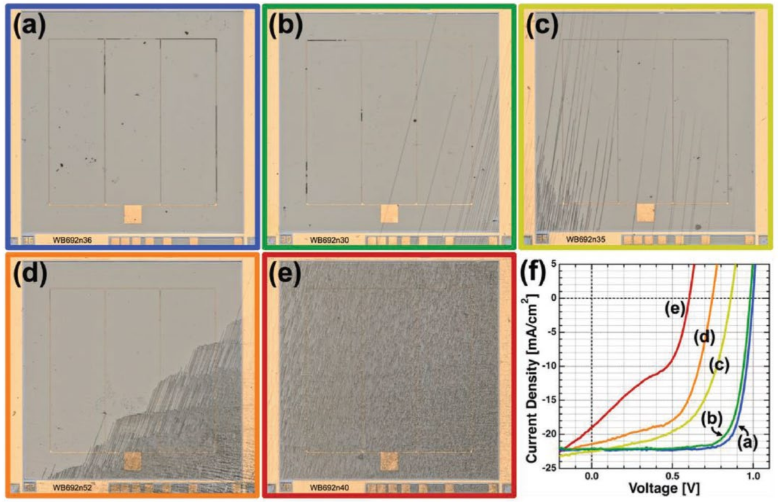
Interaction of epitaxial growth with spalled wafer surface morphology

Ge (100)



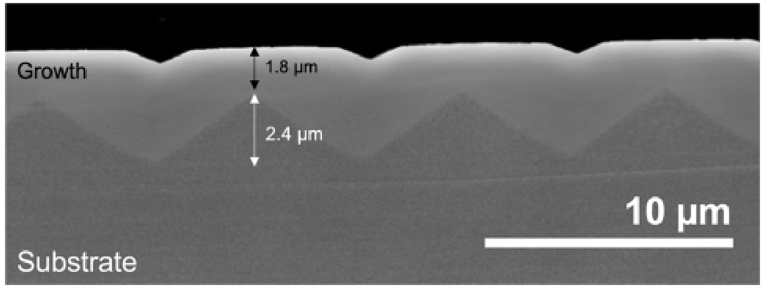


River lines are detrimental to devices, leading to dislocation nucleation and non-planarity in device layers

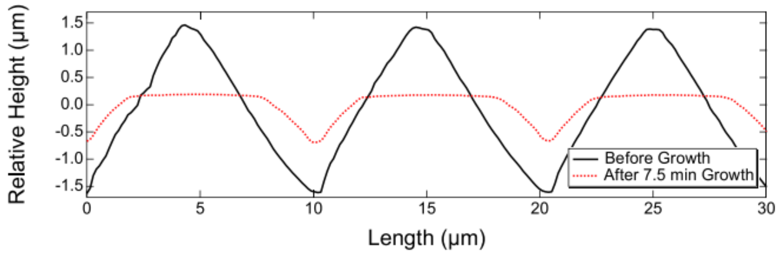


Faceted GaAs

Exploit plane-dependent growth rate anisotropy for *in situ* planarization



7.5 min of GaAs growth by HVPE



Have since achieved full planarization and followed it with device growth

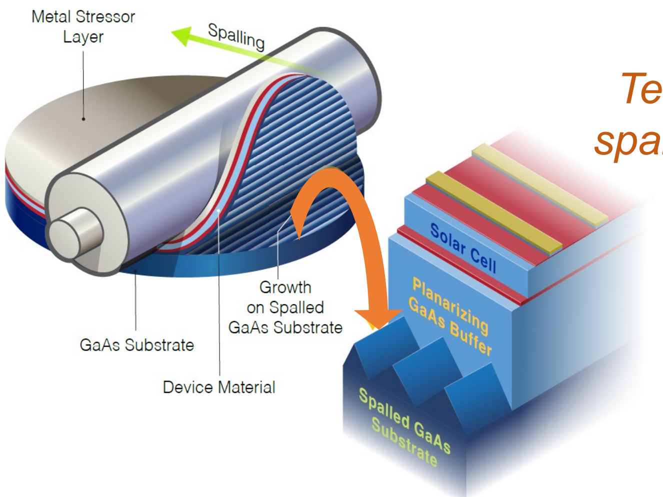
Mangum et al. *Adv. Energy Mater.* 2022

A. Braun et al. *Crystal Growth & Design* 2023

Direct reuse of wafers after spalling has promise

Wafers are spalled to mimic reuse, then device structures are grown on spalled wafer substrates, processed, and measured on wafer

Substrate Growth Method	**Device Type**	V_{OC} (V) **Spalled** Control	J_{SC} (mA/cm^2) **Spalled** Control	**Efficiency (%) Spalled** Control	**Source**
Spalled Ge (100) HVPE growth	Upright 1-J GaInPAs With ARC	**1.000** 1.002	**11.5** 10.9	**7.6** 7.4	Jain et al. 2018
Spalled Ge (100) HVPE growth	Upright 1-J GaAs No ARC	**0.900** 0.960	**18.7** 20.0	**12.8** 15.5	Cavalli et al. 2018
Spalled Ge (100) OMVPE growth	Upright 1-J GaInAs With ARC	**1.019** 1.012	**28.49** 29.38	**23.4** 23.9	Mangum et al. 2022
Spalled GaAs (110) HVPE growth	Upright 1-J GaAs With ARC	**0.915** 0.996	**21.4**	**15.6**	Metaferia et al. 2022
Spalled GaAs (100)	1-J	Coming	Soon!		



Test device on spalled substrate

PV cell performance is sensitive to material quality

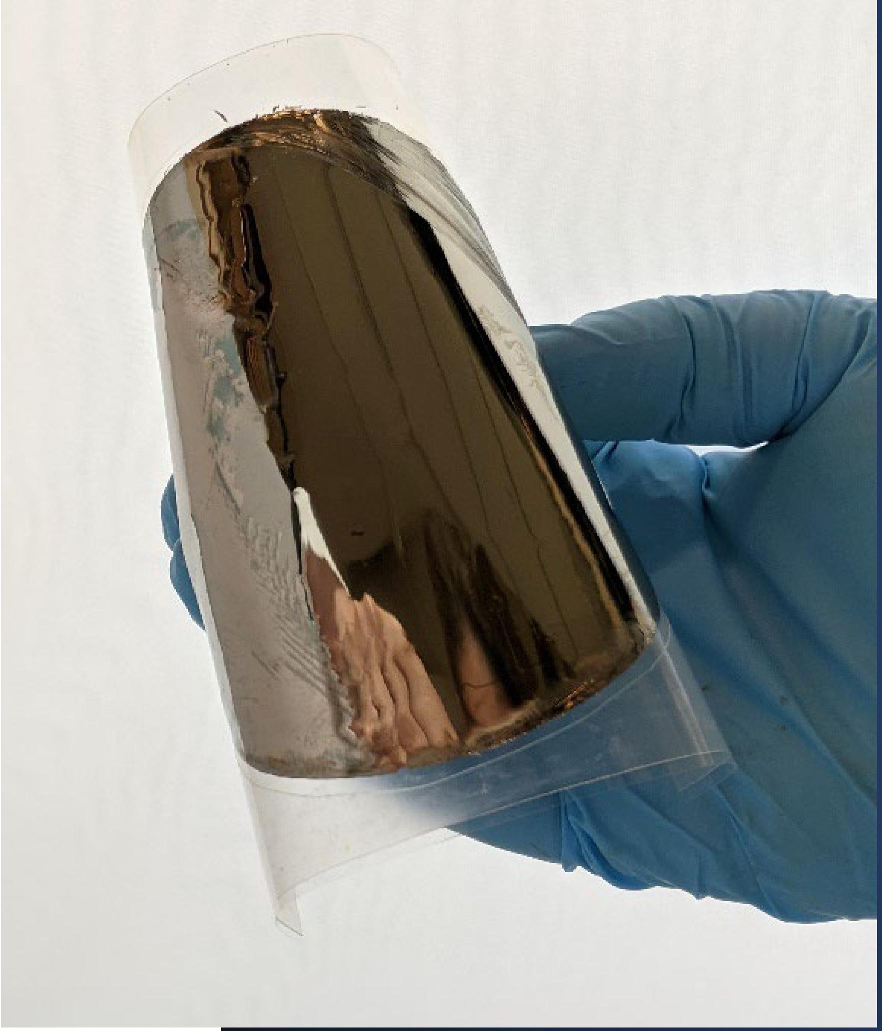
None of these substrates are polished before growth!

Morphological defects resulting from spalling can detrimentally impact growth, but high-quality devices can be grown in areas free of defects

Devices all tested under AM1.5 G 1 sun intensity (1000 W/m^2)

Summary

- Substrate reuse for III-V photovoltaic cells is an opportunity for recovering significant value
- Devices can be exfoliated from substrates without performance degradation using controlled spalling, a fast fracture-based process
- Direct reuse has significant potential; the clean surface exposed by the fracture can be a suitable surface for epitaxial growth
- Further optimization of surface morphology and growth, and process maturation are underway



All published journal articles will be made available on request
For more information, contact Corinne Packard, cpackard@mines.edu

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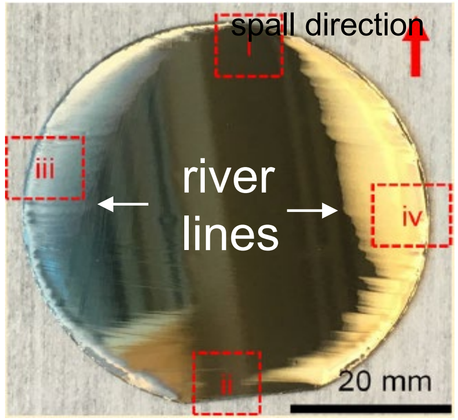
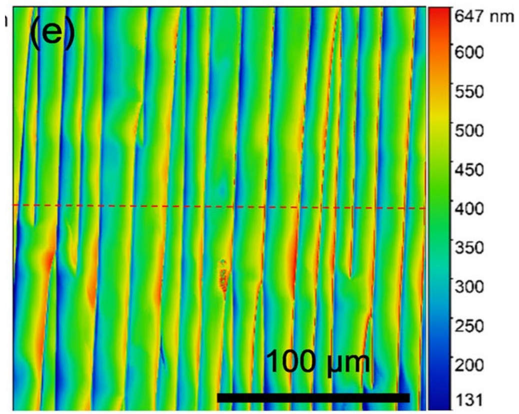
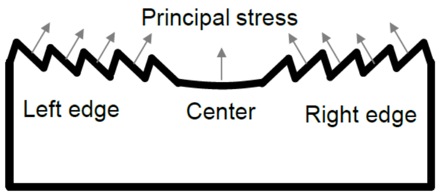
Supplemental Slides

Multiscale, cross-correlative materials characterization of root cause for performance degradation

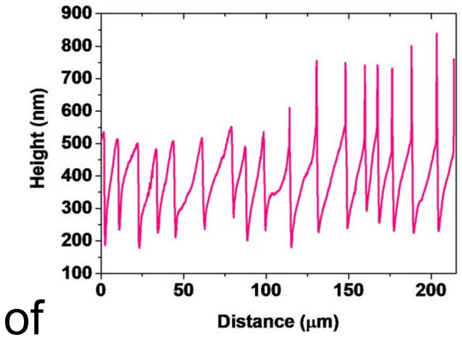
Red arrow= spall direction





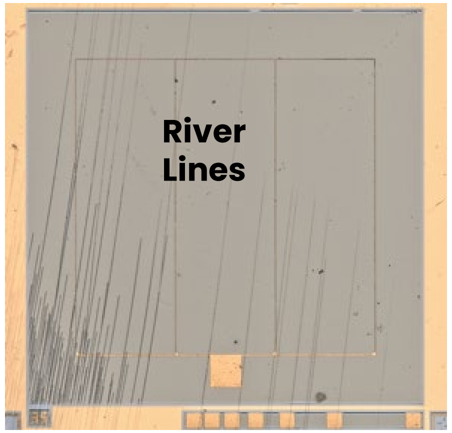


(h)

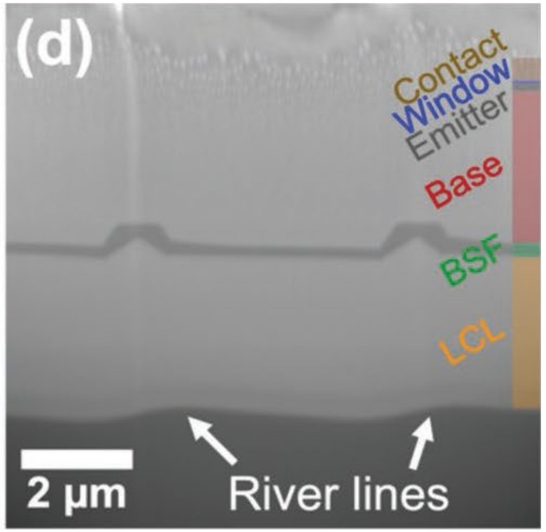


Step heights of 200nm to ~1μm

River lines cause growth disturbances and high dislocation density (~8E-7 cm^{-2})

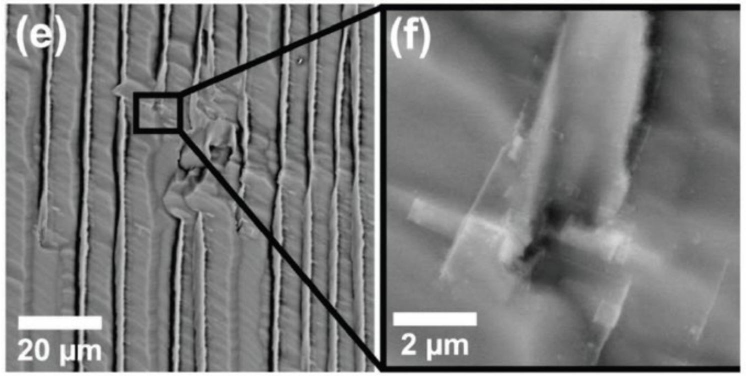


SEM cross-section



Methods:
SEM, TEM,
Photoluminescence,
Electroluminescence,
Dark Lock-In Thermography,
Electron Channeling Contrast Imaging (ECCI)

ECCI



J. Chen, J. Chenenko, and C.E. Packard, *JOM,* 2021.

Mangum et al., *Adv. Energy Mater.* 2022

Process flows for controlled spalling & processing of upright and inverted devices

Upright

Inverted

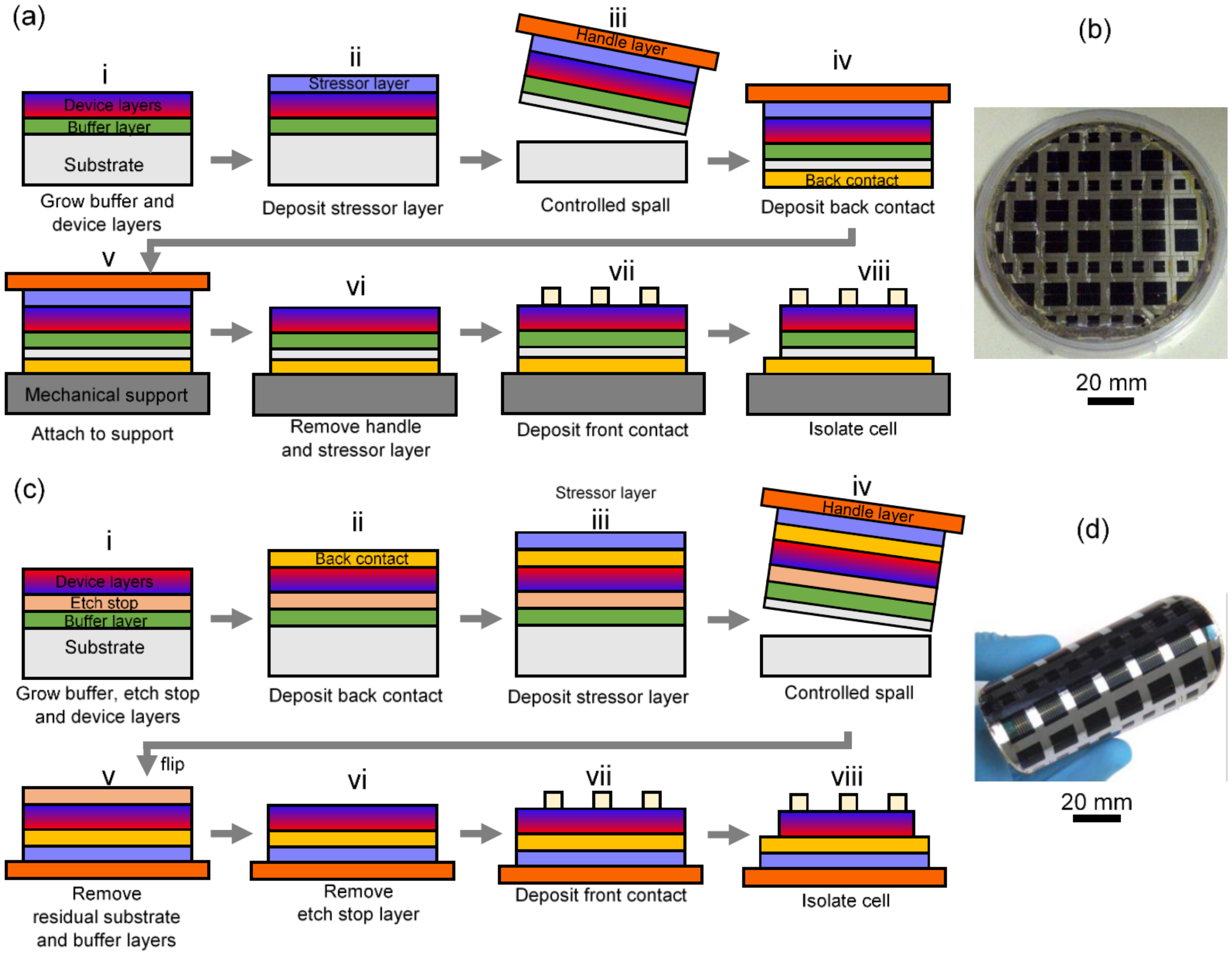
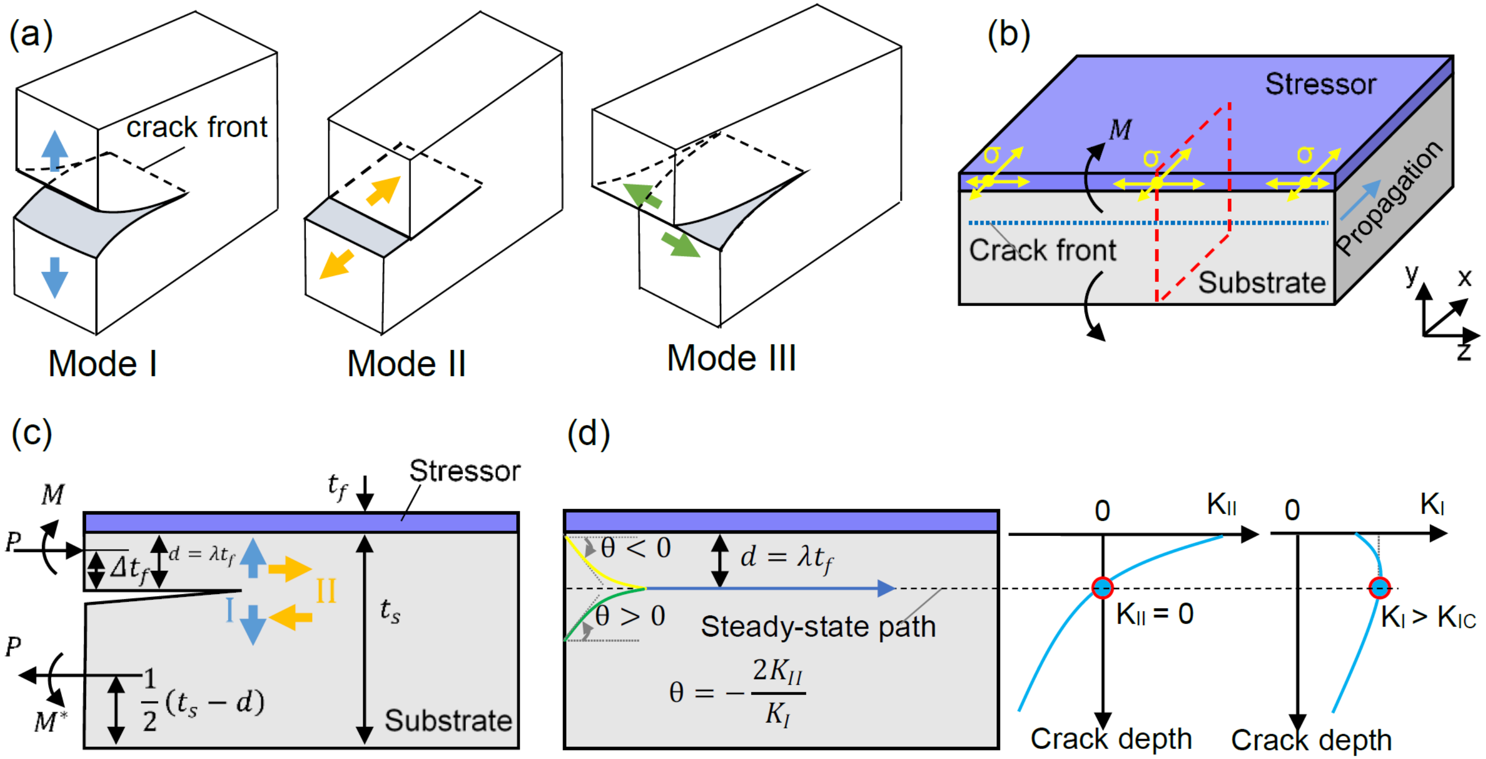


Figure & Scheme: Chen & Packard, SOLMAT 2021 https://doi.org/10.1016/j.solmat.2021.111018
Wafer photos: D. Shahrjerdi et al., ECS Trans 50 2013, and Adv. Energy Mater. 3 2013

Multiaxial Mechanics of Spalling



Chen & Packard, SOLMAT 2021

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Abstract

Wafer reuse via controlled spalling for lowering space photovoltaic cell cost

Corinne E. Packard, Aaron J. Ptak

Photovoltaic space power generation relies virtually exclusively on III-V solar technology, where the device substrate itself contributes to more than 50% of the total cell cost. The single crystal wafer substrate is necessary to achieving the highest efficiency multi-junction devices, but mostly as a growth template, with only a small fraction, or none at all, of the total wafer thickness taking an active role in power generation. Wafer reuse strategies that remove the active portion of the device while preserving the rest of the wafer for subsequent growth of another device have been identified as an important research effort to achieve cell cost-reduction. One highly promising wafer reuse strategy is controlled spalling, which propagates a stable lateral cleavage at a tuned depth in the wafer to remove the device. The cleavage fracture occurs within the wafer substrate to expose a chemically pristine surface for the first time, which we show is a suitable substrate for regrowing cells with high efficiency. This talk will highlight successful removal of high-efficiency devices, device growth on previously spalled surfaces without significant repreparation, and current limitations to the controlled spalling substrate reuse strategy.