Launch your Vision

Novel Integration of PVA String Blocking Function

27th April 2022

Novel Integration of PVA String Blocking Function

Outlook

- Overview of available solutions
- Planar blocking diode AZUR/STI design
- Thermal analysis results
- Preliminary characterization test results
- Qualification and acceptance approach

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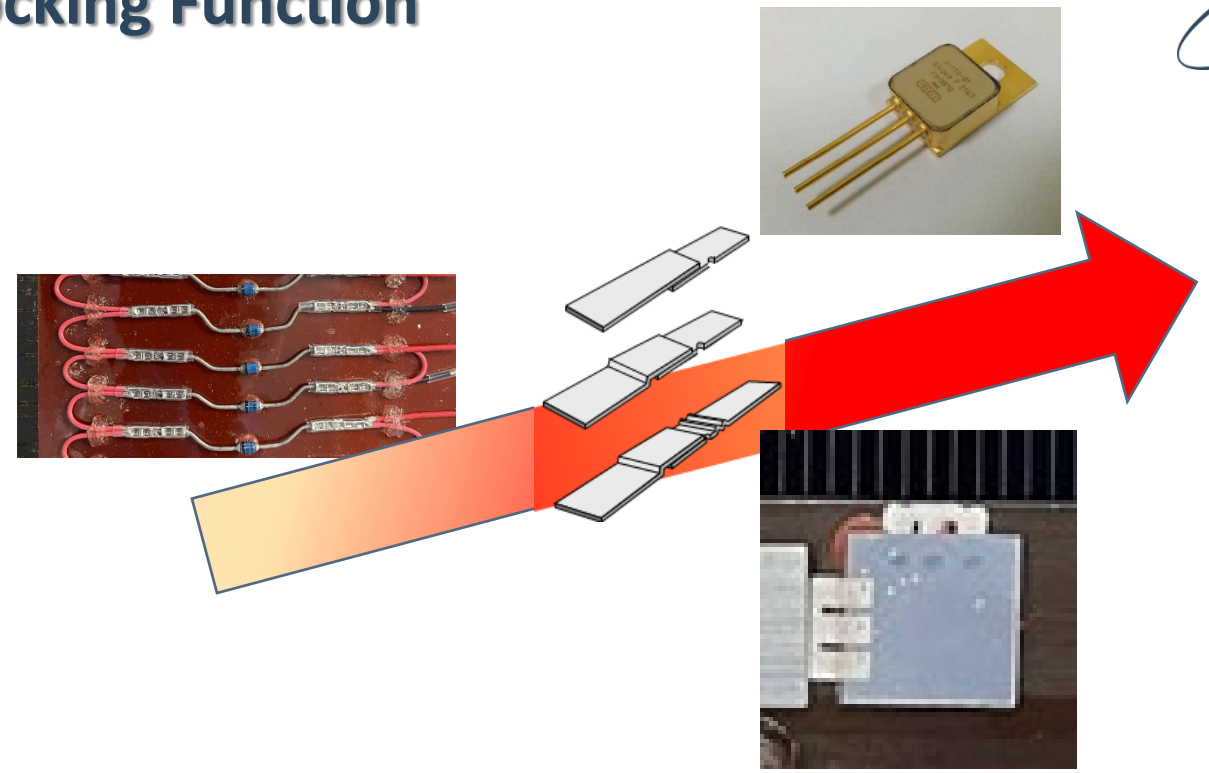
- **Example of available designs**
  - Axial diode package
  - Flex package
  - TO package
  - Silicon Planar solutions



- **Pros and Cons**
  - Temperature and current ratings
  - Suitability for the integration on deployable structures (limited clearance)
  - Design to manufacturing issues

Diode type	1NXX	Flex package	Si-C	Si Planar
Ifw max [A]	3	3	5	4
Vrev max [V]	150-400	150-400	300	400
Tj max [°C]	175	175	330	160 (TBC)
Cj-substrate [k/W]	30	5	20	5

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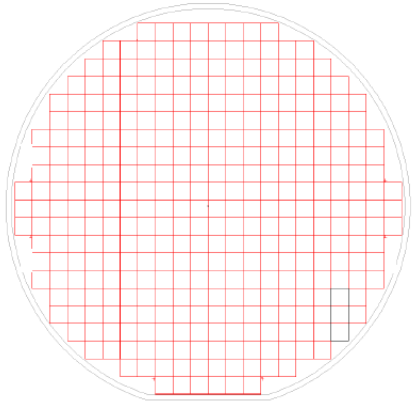
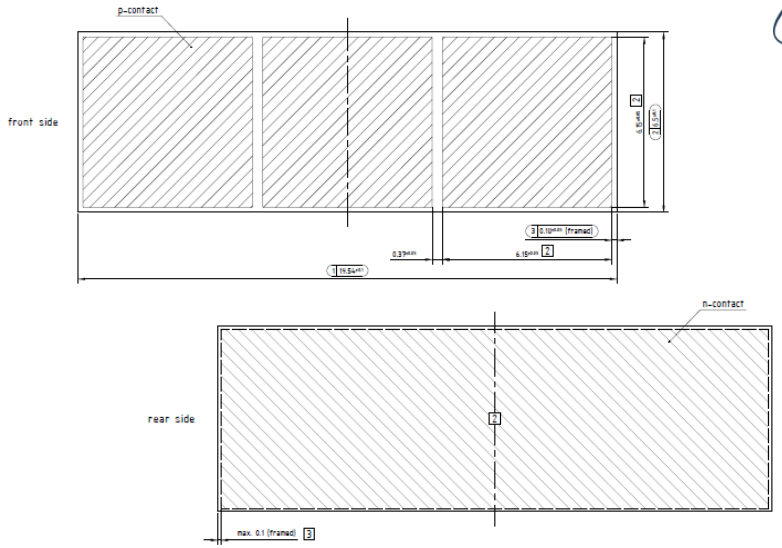
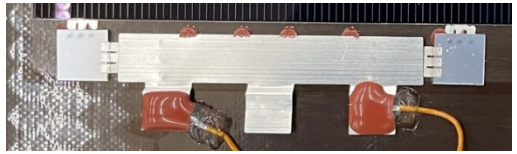
- **Basic element**
  - Device description
  - Main interfaces

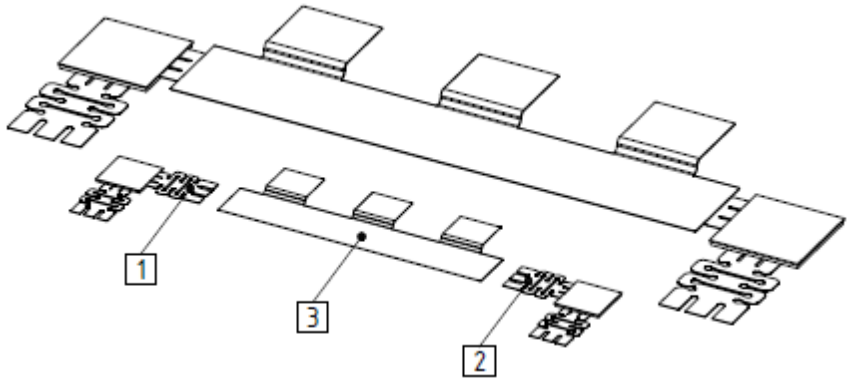


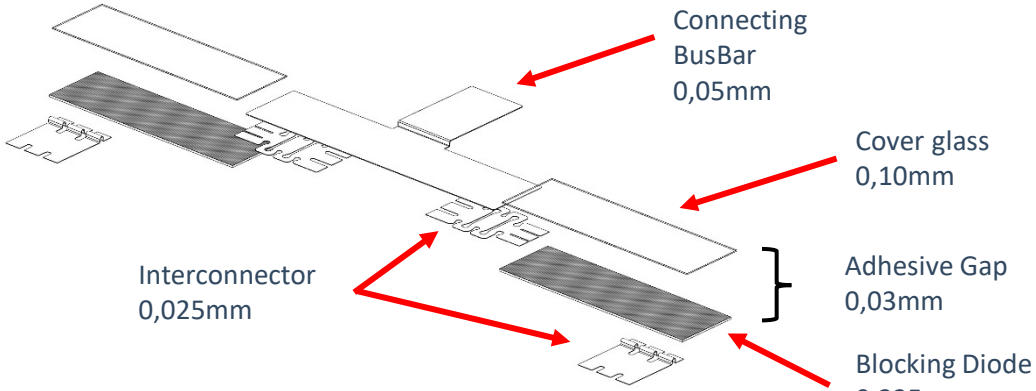
Wafer drawing with
354 single diodes (6.5mm x 6.5mm)



- **Assemblies**
  - Blocking diode assembly hints
  - Alternative solutions







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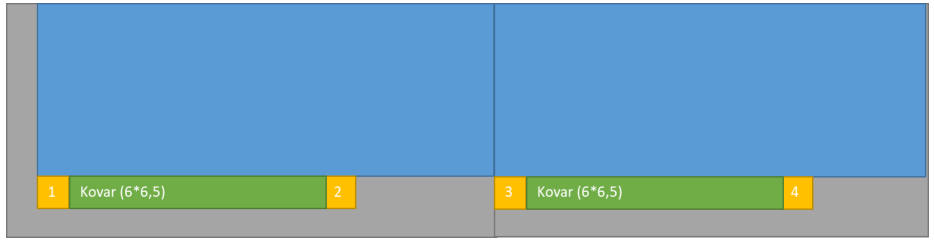
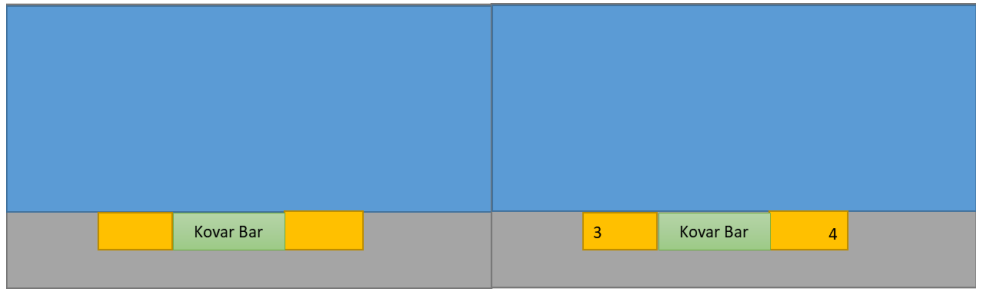
- Blocking diode configurations:

Top view:

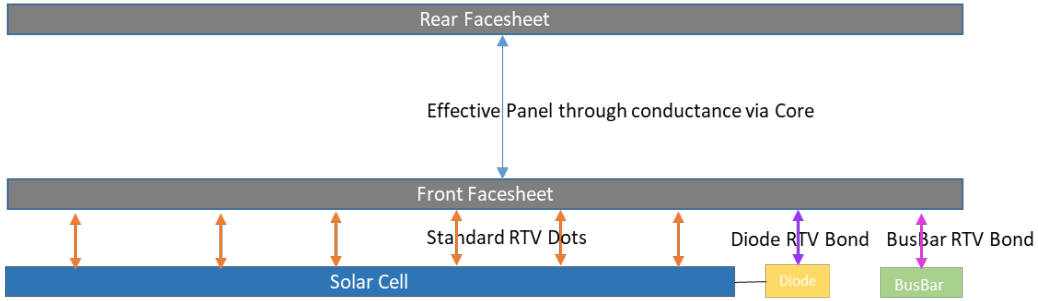


Part:	Length/mm	Width/mm
Cell	78	39
Diode	6,5	6,5
Bus Bar	39	6,5
Panel	84,5	52



Part:	Length/mm	Width/mm
Cell	123,5	58,5
Diode	19,5	6,5
Bus Bar	26	6,5
Panel	123,5	71,5

Side view:



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Boundary Conditions:

- 90° SAA
- Adiabatic panel rear side
- Environment: (worst hot assumptions)
  - Solar flux: 1423 W/m²

- Diode Dissipation (@0.5A) →

Temp. [°C]	Voltage Drop [V]	Power (W)
-40	0,78	0,39
-25	0,74	0,37
0	0,69	0,35
25	0,64	0,32
50	0,59	0,30
75	0,54	0,27
100	0,48	0,24
125	0,44	0,22
150	0,39	0,20
160	0,37	0,19
200	0,29	0,15
300	0,09	0,04

(@1,4A) →

Temp. [°C]	Voltage Drop	Power (W)
-40	0,83	1,16
-25	0,8	1,12
0	0,76	1,06
25	0,71	0,99
50	0,66	0,92
75	0,62	0,87
100	0,58	0,81
125	0,54	0,76
150	0,50	0,70
160	0,48	0,67
200	0,41	0,58
300	0,24	0,34

Sensitivity Parameters:

- Diode top surface (cover glass = SSM)
- Bus bar top surface (w & w/o cover glass = SSM)
- Conductive coupling Diode-Panel FS
- Conductive coupling Busbar-Panel FS
- Current @ diode
- Panel facesheet conductivity (in-plane FS conductivity: 46W/m/K (STI substrate design)

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PVA Front Side Diode: thermal analysis results

Baseline + Sensitivities									Temperature /°C						
Load Case #	Diode Top Surface	Bus Bar Top Surface	Bus Bar Top alpha	Bus Bar Top epsilon	Conductor Busbar - FS	Conductor Diode - FS	Current @ Diode	Diode Dissipation	Diode 1	Diode2	Diode 3	Diode 4	Busbar (max)	Cell	FS (max. @top, exposed)
14	SSM (0.2/0.8)	Ag	0,2	0,02	1x270um RTV Dot/Face	Full diode area bond	0.5A	Nominal	127,6	119,5	125,3	117,9	126	117 to 121	124,4

Load Case #	Diode Top Surface	Bus Bar Top Surface	Bus Bar Top alpha	Bus Bar Top epsilon	Conductor Busbar /QuadDiode-FS	Conductor Diode - FS	Inter-connects	Diode 1&3	Diode 2&4	QD 1&2	Current @ Diode	Diode Dissipation	Diode 1	Diode2	Diode 3	Diode 4	Busbar (max)	Cell	FS (max. @top, exposed)
Baseline + Sensitivities																			
1b	SSM (0.2/0.8)	Ag	0,2	0,02	1x270um RTV Dot/Face	Full diode area bond	Yes	On	Off	Off	1.4A	Nominal	139,9	124,7	138,2	123,0	131,6	122 to 128	132,8
	SSM (0.2/0.8)	Ag	0,2	0,02	1x270um RTV Dot/Face	Full diode area bond	Yes	1&4 Off	2&3On	Off	1.4A	Nominal	124,7	140,0	140,0	124,5	131,1	124 to 128	133,0

- Sensitivity analysis:
  - Bad coupling between diode and substrate (> 80K)
  - Reduced substrate in plane thermal conductance (5 -10K)
  - Increased diode radiative surface (5 -10K)
  - Influence of the coverglass (SSM) (3 -5K)
  - Influence of the interconnects (3 -5K)

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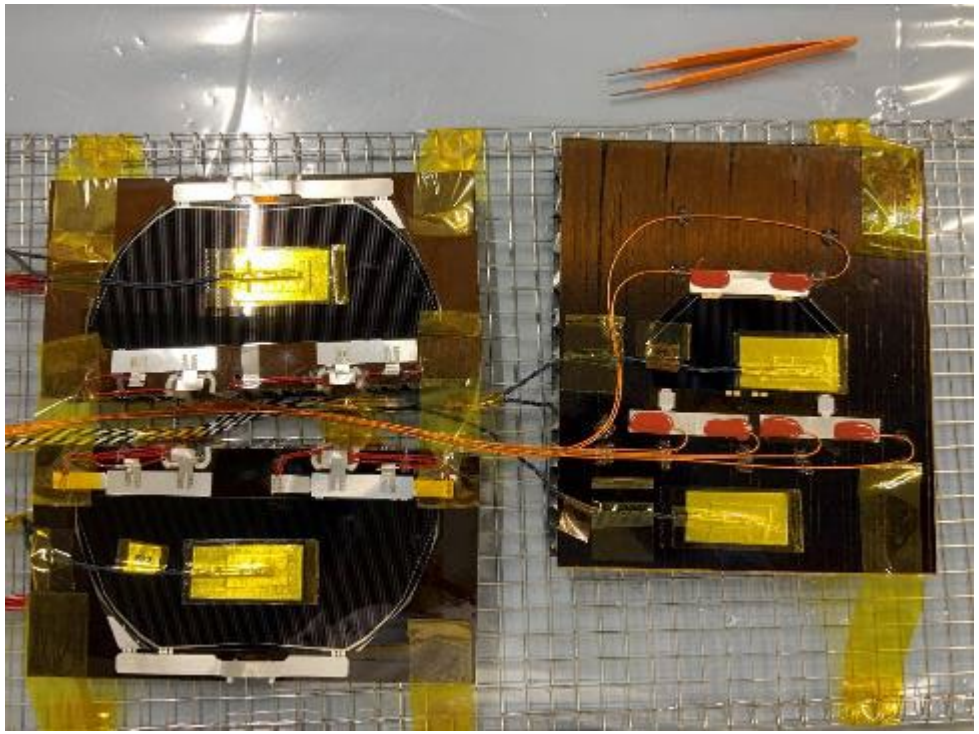
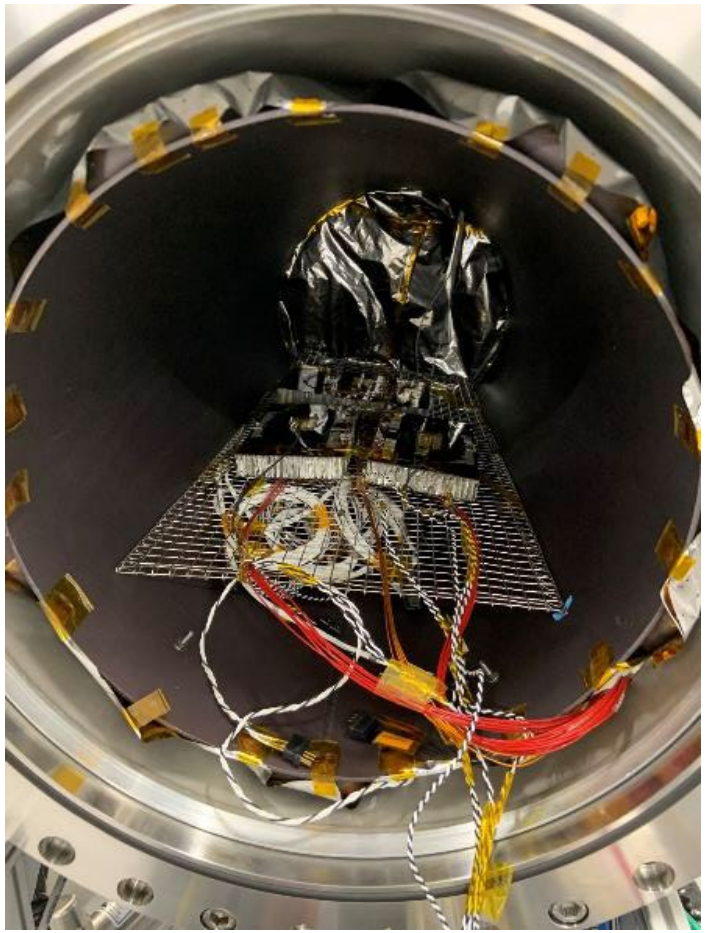
Preliminary characterization test results





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Preliminary characterization test results

Calibration phase

- Forward bias pulsed and reverse bias continious mode measurements at temperatures:

T1: -150°C (-0 /+5°C)
T2: -130°C (-0 /+5°C)
T3: -100°C (-0 /+5°C)
T4: -40°C (-0 /+5°C)
T5: -25°C (-0 /+5°C)
T6: 0°C (-0 /+5°C)
T7: 50°C (-0 /+5°C)
T8: 75°C (-0 /+5°C)
T9: 100°C (-0 /+5°C)
T10: 125°C (-0 /+5°C)
T11: 160°C (-0 /+5°C)

- Forward bias continious and pulsed conditions compared to identify heating effect of measurement
- Two different pulse durations were investigated to identify heating effect during measurement (Azur Space reported a similar issue found during preliminary tests)

Forward bias characterization

- Continuous forward biasing of blocking diodes min. 5 minutes until stabilization of V_{FWD} at temperatures

T12:-150°C (-0 /+5°C)
T13: 75°C (-0 /+5°C)
T14: 100°C (-0 /+5°C)
T15: 125°C (-0 /+5°C)
T16: 160°C (-0 /+5°C)

- Comparison of parallel vs single diode behaviour
- Evaluation of the diode juncion temperature by comparing the forward voltage with the calibration curves previously taken

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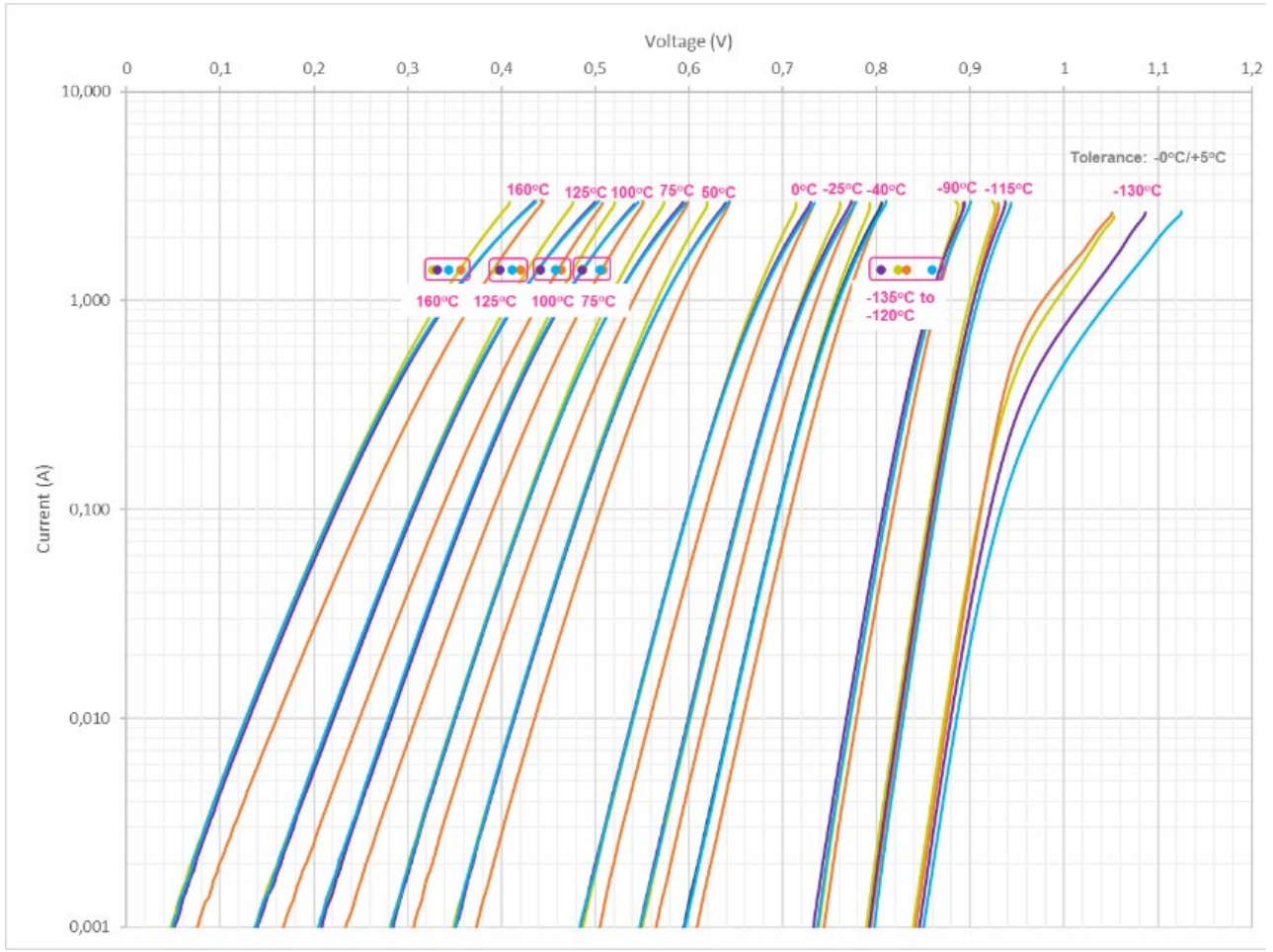
Preliminary characterization test results

Results of first TV tests confirmed that

- 230µm thickness (about cell thickness) results in sufficient heat spreading function, even if one of the 2 parallel diodes have failed. Nevertheless, thermal design and fatigue lifetime of a diode is just qualified with 2 active diodes while targeting robust margins
- Under extreme hot temperatures (150°C housing, about +5/+10°C on the junction at 0,7 and 1,4A) for a single diode the voltage drop of a parallel diode assembly was measured below 0.36 V at a max current of 1.4 A (corresponding to a half pipe 3G30 cell with about 80 cm^2), resulting in a PDA thermal dissipation of < 0.5 W



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Preliminary conclusions

Diode rating

- Likely higher than the announced 150°C junction temperature

Diode configuration

- Single diode compatible to large cell power dissipation
- Planar blocking diode has the advantage of reduced operational temperature, hence improve reliability

Overall diode performances

- Sufficient to cover a wide range of missions
- Lifetests should be performed asap in order to increase confidence

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- **Design and qualification standard coverage**
  - European E-20-08 is currently under revision to incorporate novel blocking diode designs
  - ESCC-5000 and ECSS guidelines were used to define a suitable test approach
  - The heritage cumulated in the last 20 years on the Silicon planar bypass diode was as well considered
  - Similar qualification approach as followed on Si planar bypass diode

- **Acceptance testing approach**
  - Early screening at wafer level
  - High temperature forward and reverse testing on 100% of the devices (high temperature reverse bias)

- **Qualification subgroups**
  - Bare diode (with interconnectors for easying the electrical contact)
  - Blocking diode assembly (planar diode assembly – PDA)

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Qualification hints

Subgroup	Specimen q.ty	Test scope	Test hints
O **group 1 bare diodes, group 2 blocking diode assemblies**	Group 1 20 + 5 spare Group 2 20 + 5 spare	Extended storage simulation	HT1: 30 days, 60 °C, ≥ 90 %RH CY: 640 cycles from -80 °C to +150 °C IA: 45°: ≥ 5 N
V **Bare diodes plus front and rear side interconnects**	20 + 5 spare	Long duration life test	Power burn-in Tjunction = 160 °C, Duration: 96 h, IFwd = 4 A High temperature Reverse burn-in Tjunction = 160 °C, Duration: 200 h, VRev = 300 V Long duration life test 4000 hrs @ 175°C & 185°C (50% -50%)
C **group 1 bare diodes, group 2 bare diodes plus front and rear side interconnects**	Group 1 24 + 6 spare Group 2 24 + 6 spare	Radiation testing	Power burn-in Tjunction = 160 °C, Duration: 96 h, IFwd = 4 A High temperature Reverse burn-in Tjunction = 160 °C, Duration: 200 h, VRev = 300 V Temperature behaviour & Temperature robustness Total Dose radiation testing Ionising radiation (Co60) 50 Mrad; Non ionising (electrons): 1MeV
A **bare diodes plus front interconnector**	20 + 5 spares	Contact Adherence front	Surge test: 10 pulses @ Imax Human body ESD 12 kV single and multi-pulse CY 640 cycles from -80 °C to +150 °C IA 45°: ≥ 5 N
E **bare diodes plus front, rear interconnector and coverglass**	20 + 5 spares	Contact Adherence rear	Surge test: 10 pulses @ Imax CY 640 cycles from -80 °C to +150 °C IA 45°: ≥ 5 N

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Conclusions

- **Applicability of the Si planar blocking diode solution**
  - Depending on the available area surrounding the diode and in-plane dissipation
  - Suitable for deployable rigid arrays
  - To be further assessed for flexible roll out structures
  - Close to the limit for adiabatic mounting
- **Running qualification activities**
  - Full qualification running in the frame of ESA PLATO PVA (L2 adiabatic)
  - Delta qualification foreseen for covering standard LEO and GEO environments
- **Flight model implementation**
  - Under qualification in the frame of ESA PLATO mission (expected launch date on 2026)
  - Baseline for ESA Copernicus missions managed by STI (expected launch dates from 2026 on)
- **In orbit heritage**
  - A first planar blocking diode concept is flying since mid-2019 on board of YORK SA (8x8 TJ cells)

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