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Early Successes with GaN in AEPS (Advanced Electrical Power Subsystem) DC-DC Regulators at NGAS

Space Power Workshop 2019

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NGAS, Redondo Beach, Calif.

Presentation Overview

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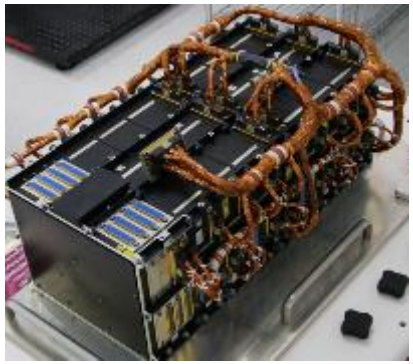
- AEPS Products: Quick Overview
- Motivation for GaN Insertion, Relative to AEPS Products
  - Development timeline
  - Ground rules to control risk/scope
- Progress Report: Successes with 500W GaN Breadboard Regulators
  - Parts selected
  - Board design for paralleled GaN FETs
  - New capabilities in test equipment / diff probes / oscilloscopes
  - Waveforms, Test Data, and Photos from the 500W regulator breadboards
- Next Steps towards flight design insertion

GaN adoption proceeding at a steady pace within AEPS Products

AEPS Products: Quick Overview

- Advanced Electrical Power System (AEPS) is the DC-DC conversion link between satellite solar array, battery, main bus, and payloads
  - All spacecraft power passes through these units
  - Power Control Unit (PCU), Battery Charge + Discharge Unit (BCDU)
  - Provides programmable, tightly regulated bus voltage (32.5V to 34V), programmable battery charge control, solar array peak power tracking, metering and distribution of bus power, digital processing of CMD/TLM via MIL-STD-1553
  - Expandable in 1000W blocks due to modular design
  - Approx 95% DC-DC conversion efficiency

PCU UNIT



BCDU UNIT

Goal: Insert GaN FETs into an established product line, controlling scope of design changes to minimize new risk

AEPS Products: Quick Overview

- PCU regulates the *load* section of solar array via buck regulators, and contains the “main bus” which is distributed out to the spacecraft

- One or more BCDUs regulate the charge section of solar array sections to charge batteries (via buck regulators) during sunlight, and provide regulated power to the main bus (via boost regulators) in eclipse

- Both units contain the following slices
  - **Series-Switched Electronics (SSE):** Buck Regulator 2x500W per slice
  - **Battery Discharge Electronics (BDE):** Boost Regulator 2x500W per slice

  GaN target
  - **Regulator Error Amplifier (REA):** Error Amplifier slice (PCU, Array and Battery)
  - **Digital Input / Output (DIO):** Command & Data Handling slice
  - **Battery Interface Electronics / Power Distribution Module (BIE/PDM):** Low impedance interface and fused distribution nodes for spacecraft bus/battery

AEPS GaN Insertion: Motivation

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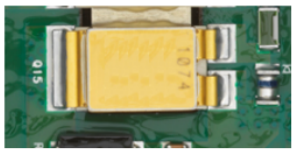
- **Key advantages, relative to radhard Si, from GaN higher bandgap energy and higher electron mobility:**
  1. Lower Rds-on -> lower conduction loss -> **more efficient**
  2. Lower Gate Charge -> lower gate drive loss -> **more efficient**
  3. Faster Switching Transitions -> lower switching loss -> **more efficient**
  4. Physically smaller transistors for a given Rds-on > **more automated board assembly**
  5. Higher switching freq capability -> smaller LC filters -> **potential to reduce box size**

Going after #1-4 first

	Existing SSE/BDE FET	Proposed GaN Alternative
Voltage	200V	200V
Drain current	53A	18A (use 3 in parallel for 54A)
Total gate charge (lower is better)	155nC	6nC (3 in parallel = 18nC)
Rds-on (lower is better)	38mohm Rdson	26mohm (3 in parallel = 9 mohm
TID (higher is better)	100krad	300krad
Size (in)	0.70 * 0.53 * 0.15 high body only (leads extra) (inches)	0.22 * 0.15 * 0.09 high (3 in parallel = still smaller than one SMD-2 (inches)
		

GaN FET outperforms significantly on key metrics

AEPS GaN Insertion: Ground Rules

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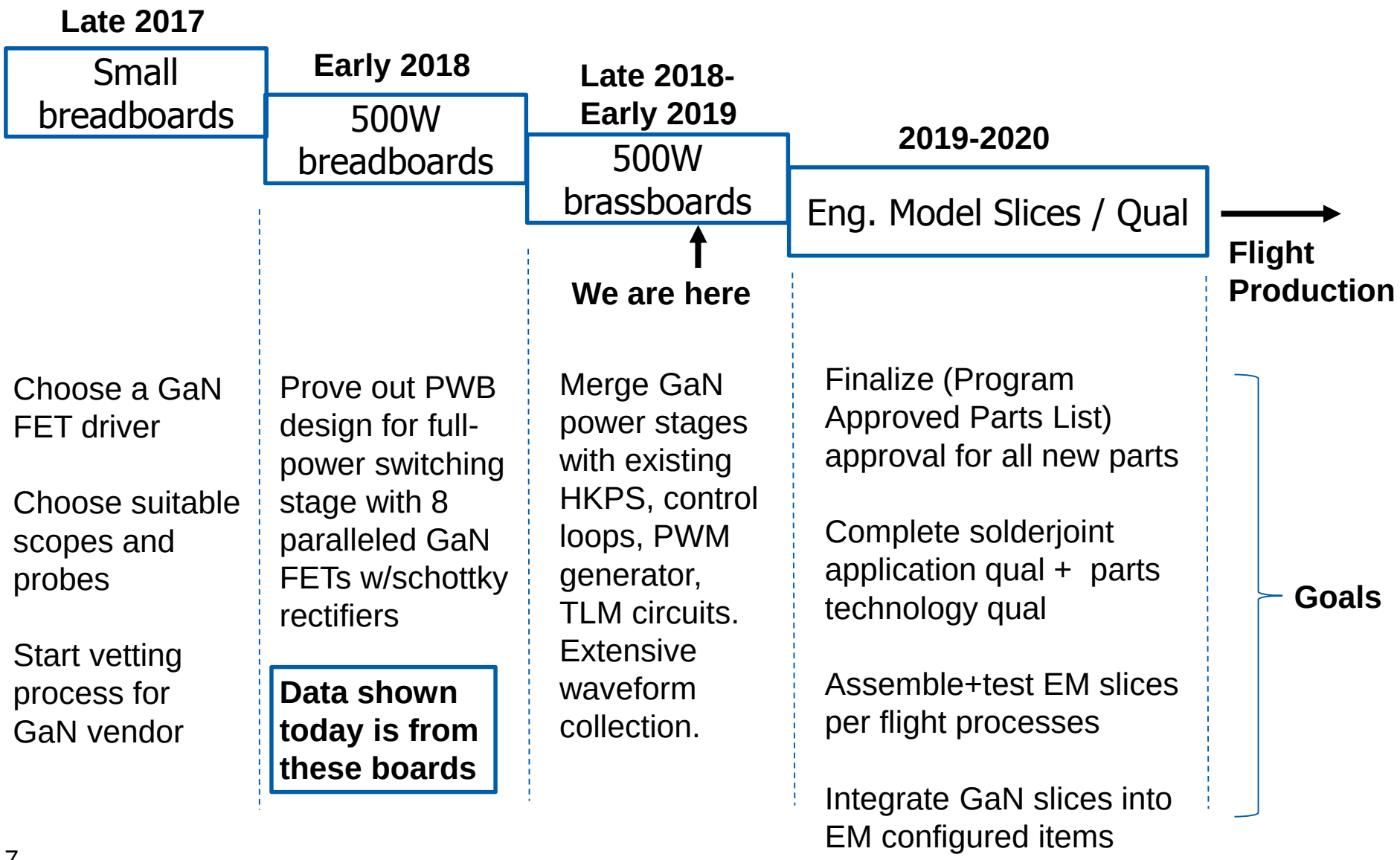
- **AEPS approach: Control scope to limit the amount of redesign and new risk, for 1st generation of GaN-enabled regulators**
  - **Keep switching frequency the same**
    - No change to continuous-mode dynamic transfer functions
      - Minimizes impact to stability and transient response analysis
    - Maximizes efficiency gains
    - Maximizes reuse of existing LC filters, current monitors, loop compensation
  - **Form/fit/function of regulator slices unchanged**
  - **Limit GaN insertion to main switching transistors; still using RH Si FETs for numerous support circuits**
  - **Intent is to capture higher efficiency and increased producibility, while being mindful of tradeoffs** (no avalanche capability, sensitivity to PWB layout, reduced Vgs voltage margins, Qual risk, EMC risk)

AEPS GaN Insertion: Timeline



AEPS GaN Insertion: Board Comparison

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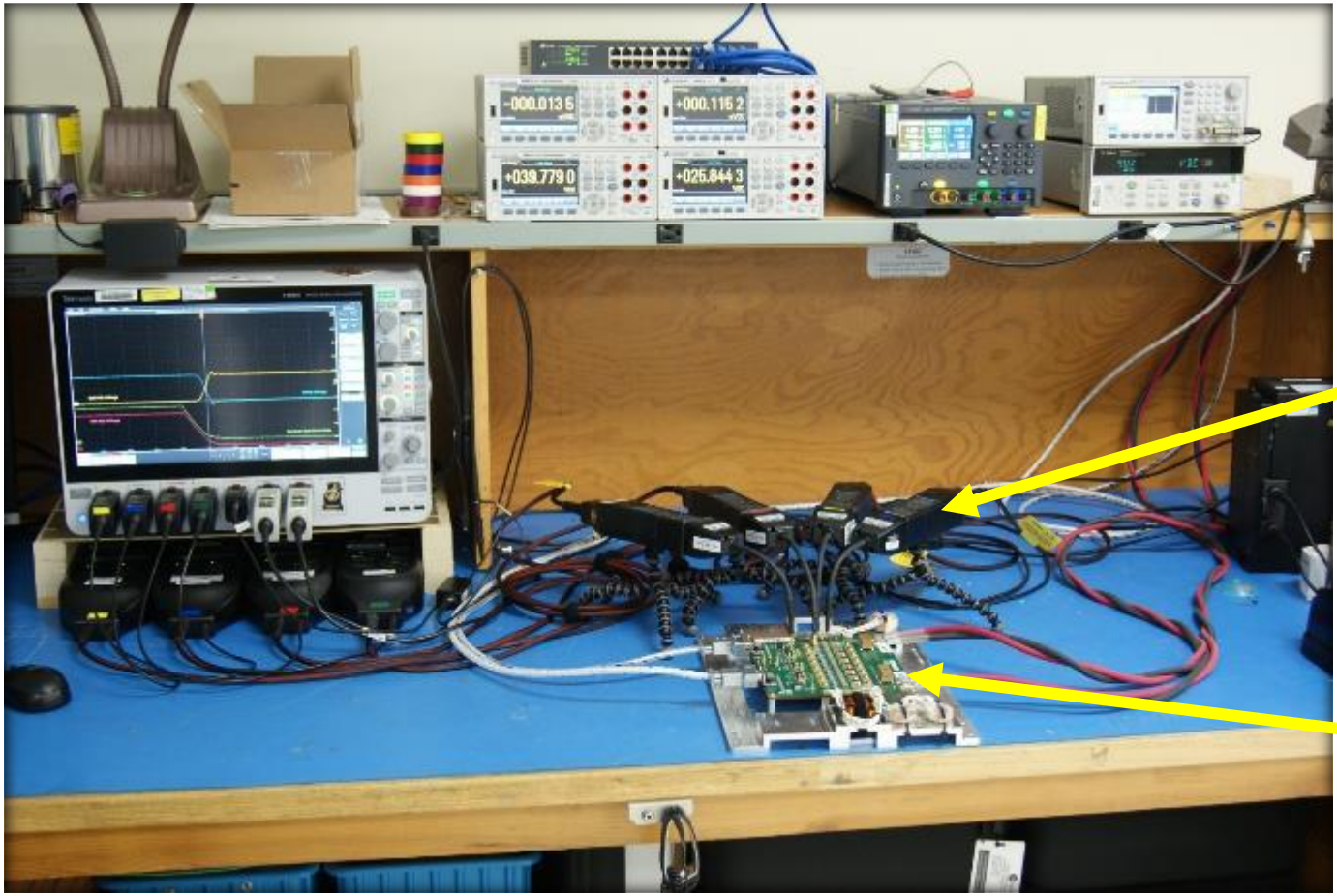
- 4x large MOSFETs, mounted with direct thermal path to chassis (raised pedestal protruding through board)
- Required manual soldering and thermal bonding of FETs
- Due to off-board FET mounting, less optimal PWB layout

Heritage Design

- 8x small GaN HEMTs, mounted directly on circuit card (changed diodes to match as well)
- Machine installation; manual soldering and thermal bonding steps eliminated
- No cutouts in board: able to optimize board for low inductance electrically

New GaN Power Stage Breadboards

AEPS GaN Insertion: Test Bench

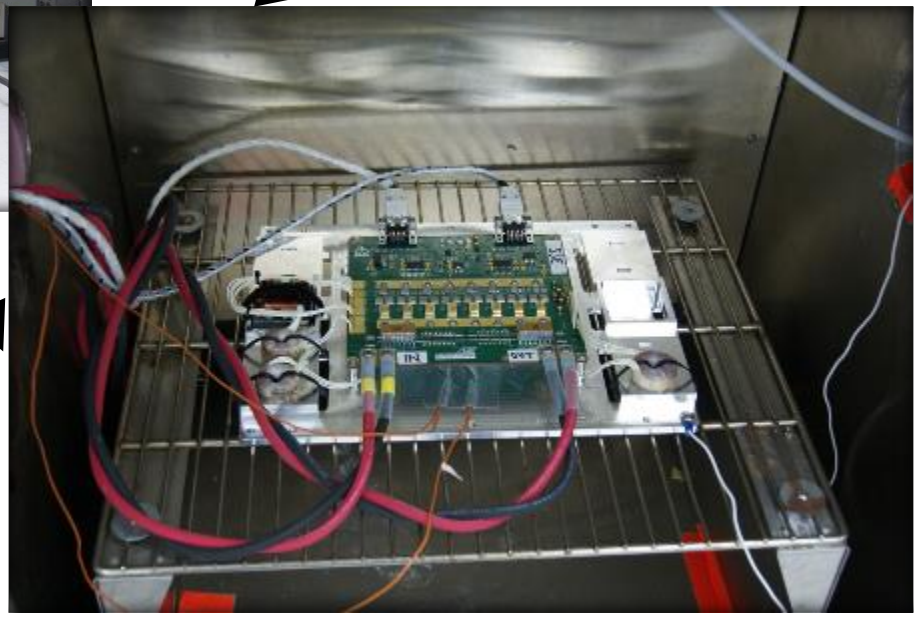


High speed differential probes necessary for GaN waveform collection

Power stage breadboard

AEPS GaN Insertion: Test Bench

Temperature tests conducted



AEPS GaN Insertion: Test Bench

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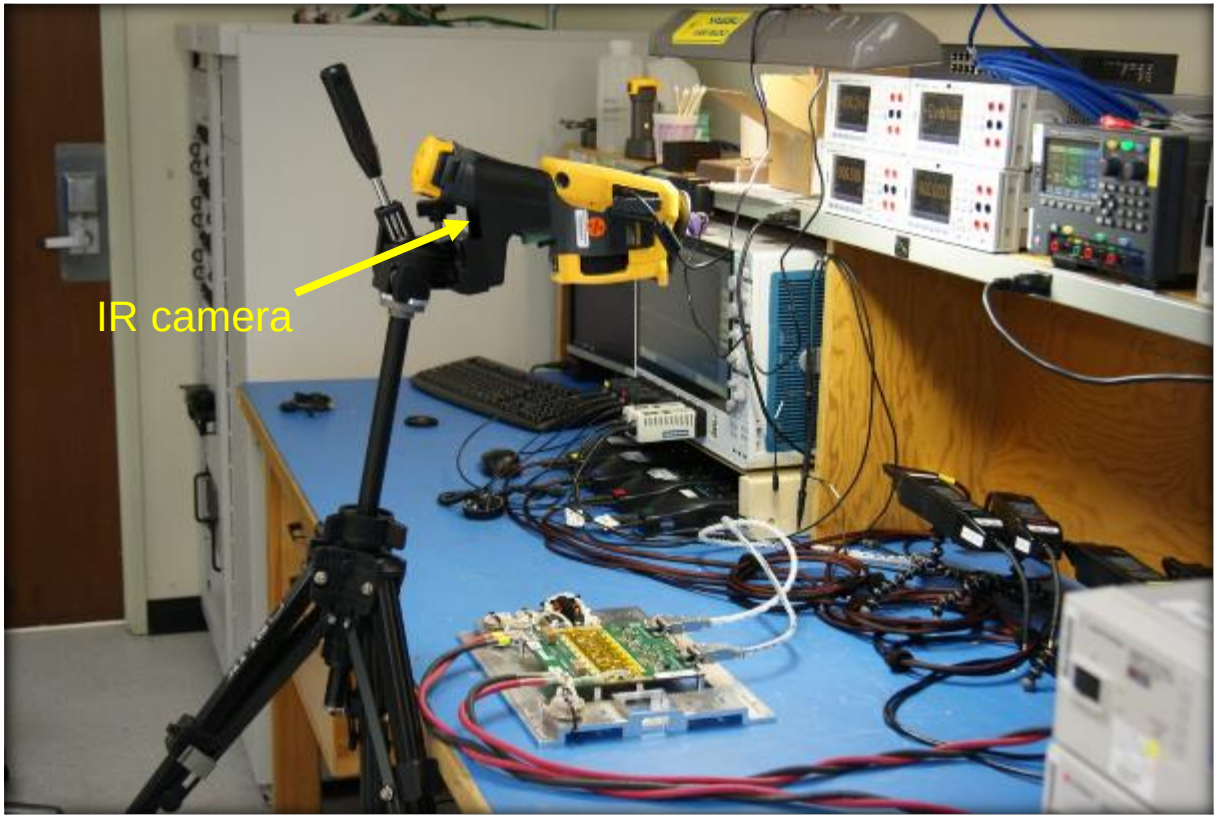
Infrared Thermography:

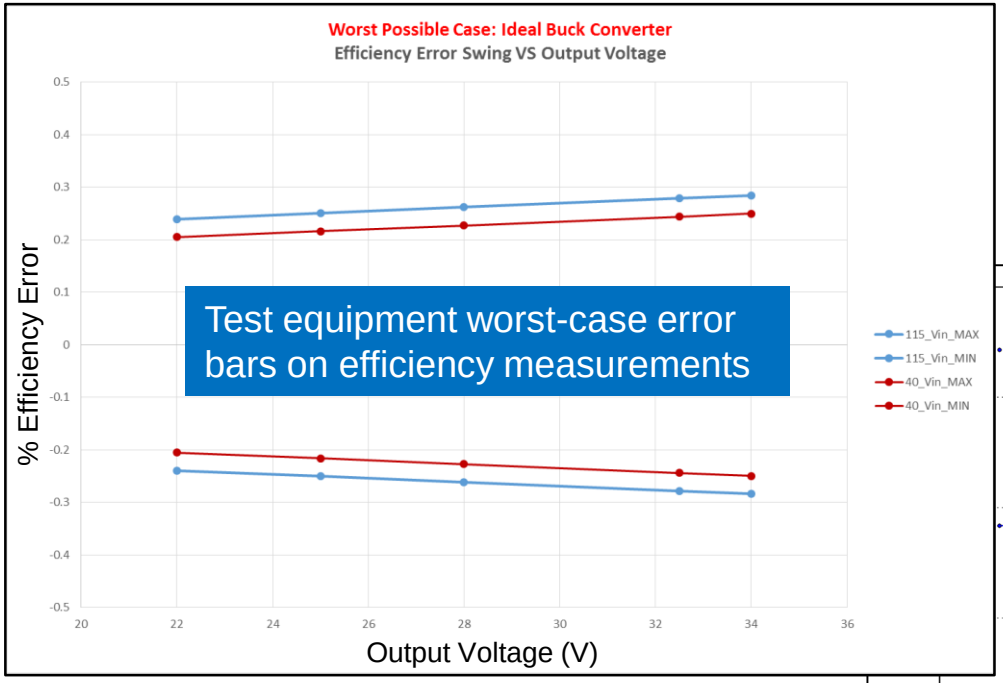
#1 to confirm good current sharing between paralleled GaN FETs

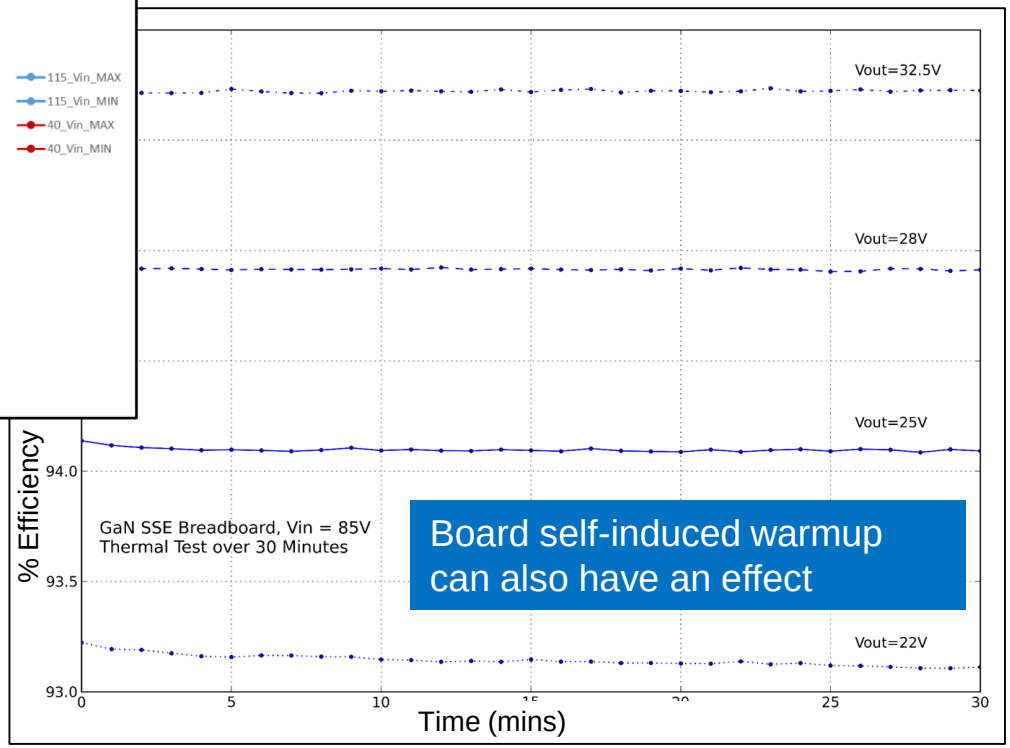
#2 To anchor thermal analysis



#3 Gain confidence in new board design with FETs and diodes on PWB

AEPS GaN Insertion: Test Setup





Accurately measuring GaN efficiency improvements requires careful management of test tolerances

AEPS GaN Insertion: Breadboard Results

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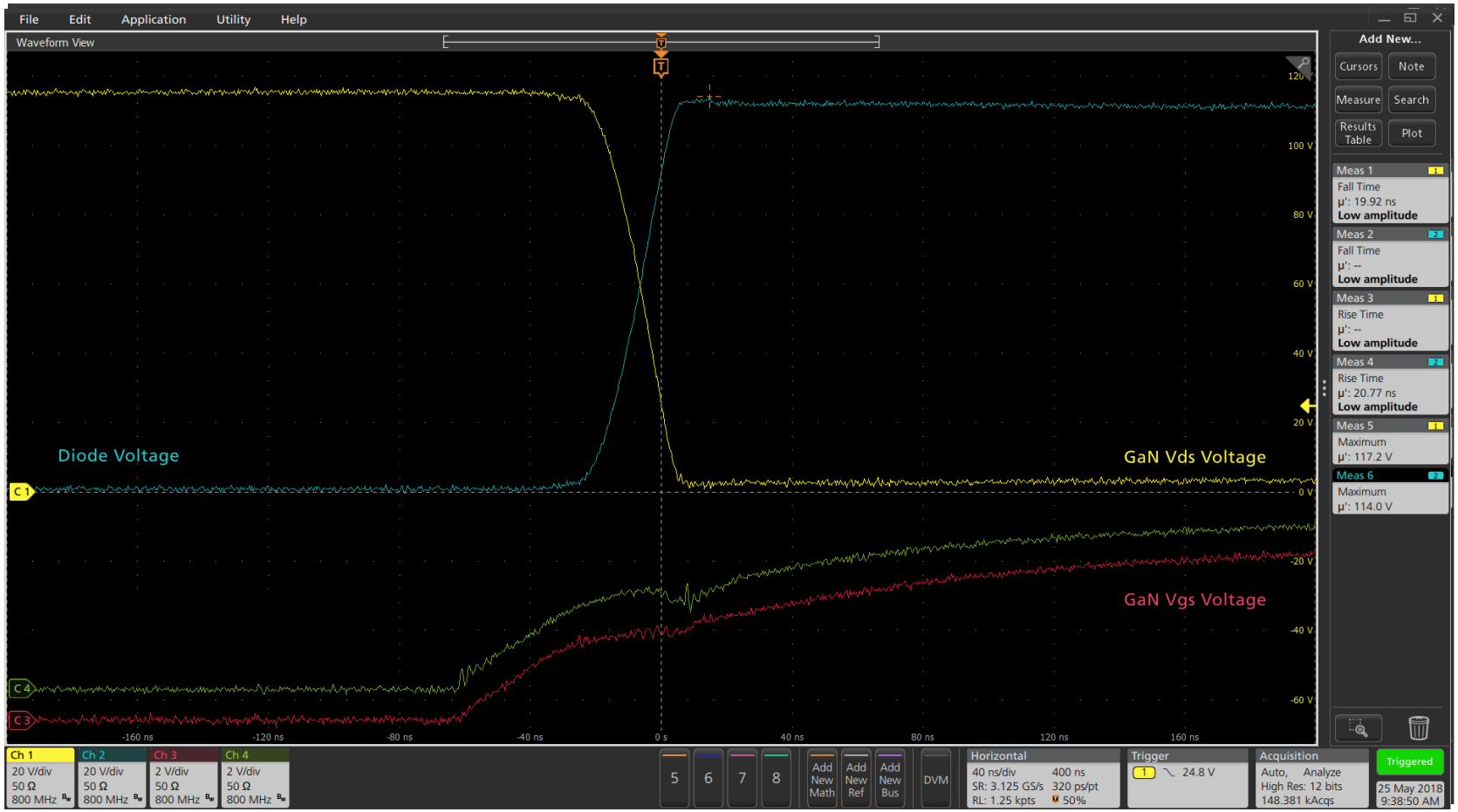
The AEPS GaN breadboard effort successfully completed the planned goals:

- Reduce board layout risk (demonstrated low inductance and safe voltage stresses on high-speed GaN HEMTs)
- Show part temperatures are acceptable via preliminary thermography
- Demonstrate increased manufacturability due to machine-installable GaN parts
- Demonstrate increased efficiency
- Surprises: GaN transistor and Schottky diode waveform stress turned out better (less ringing) than expected, due to such high focus applied to PWB design

Breadboard effort achieved stated risk-reduction goals

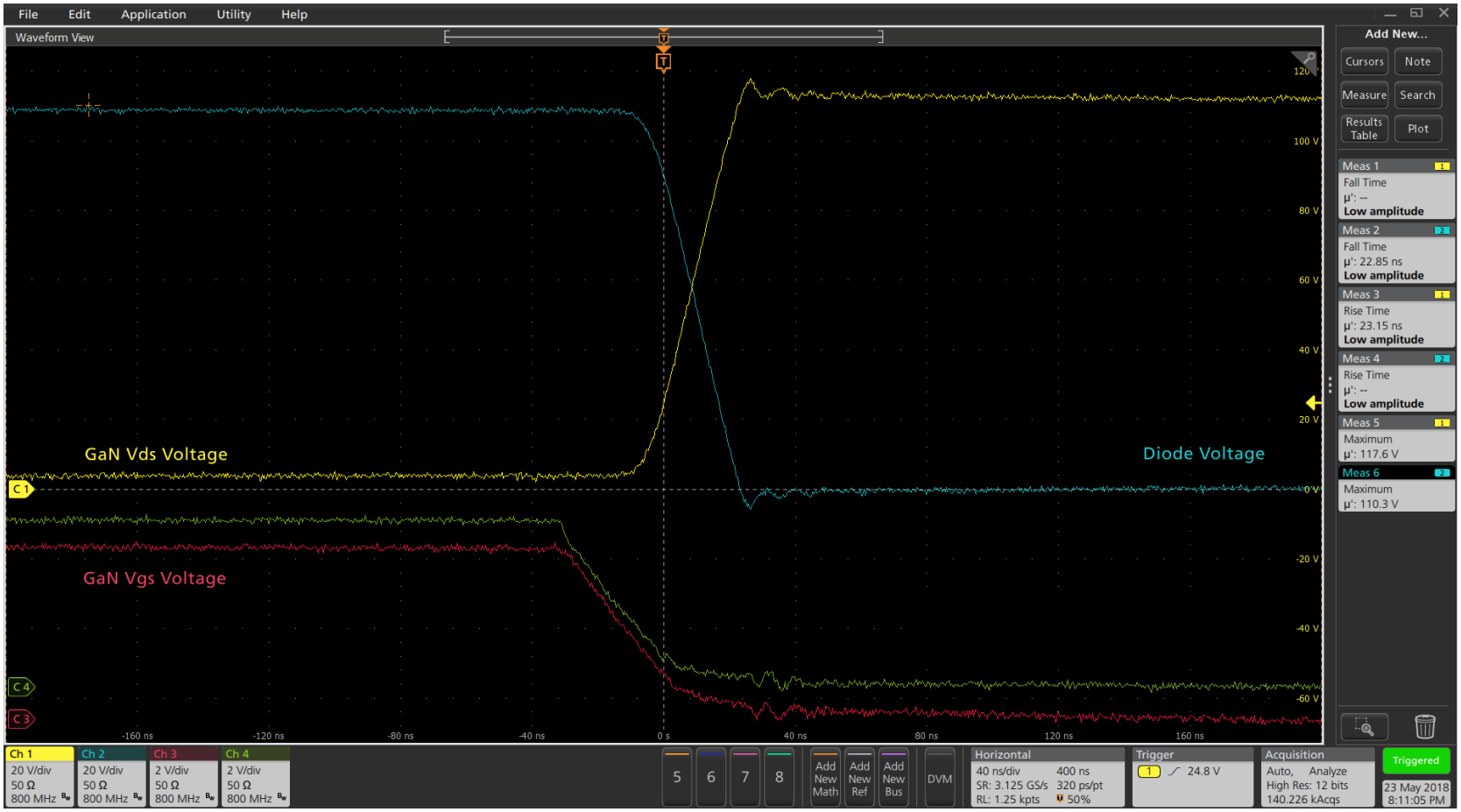
AEPS GaN Insertion: Breadboard Results



Buck FET Turn-On Stress Waveforms (115V in/ 22V out/500W out)

Better than expected: Very low overshoot on GaN FET Vgs and Vds waveforms

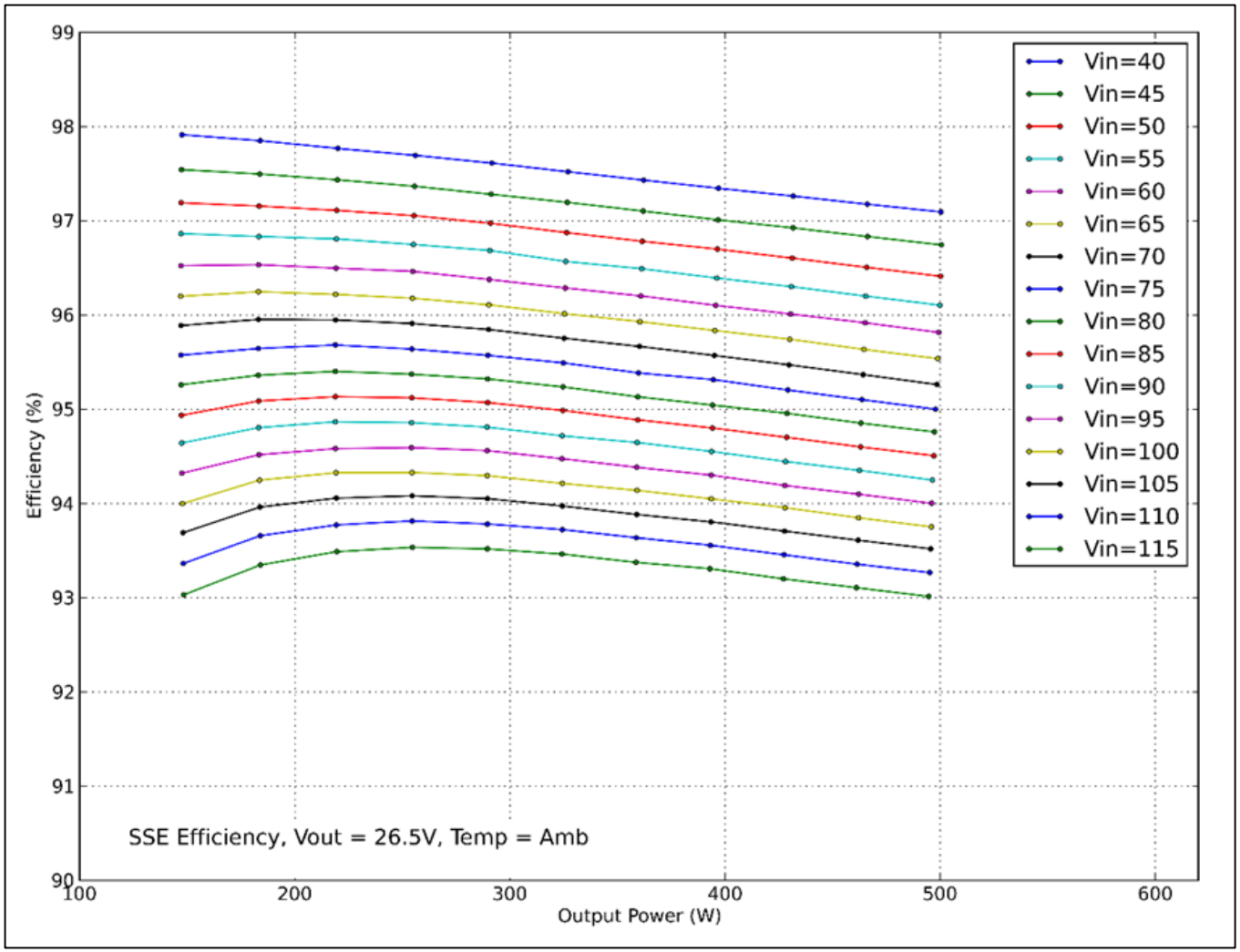
AEPS GaN Insertion: Breadboard Results



Buck FET Turn-Off Stress Waveforms (115V in/ 22V out/500W out)

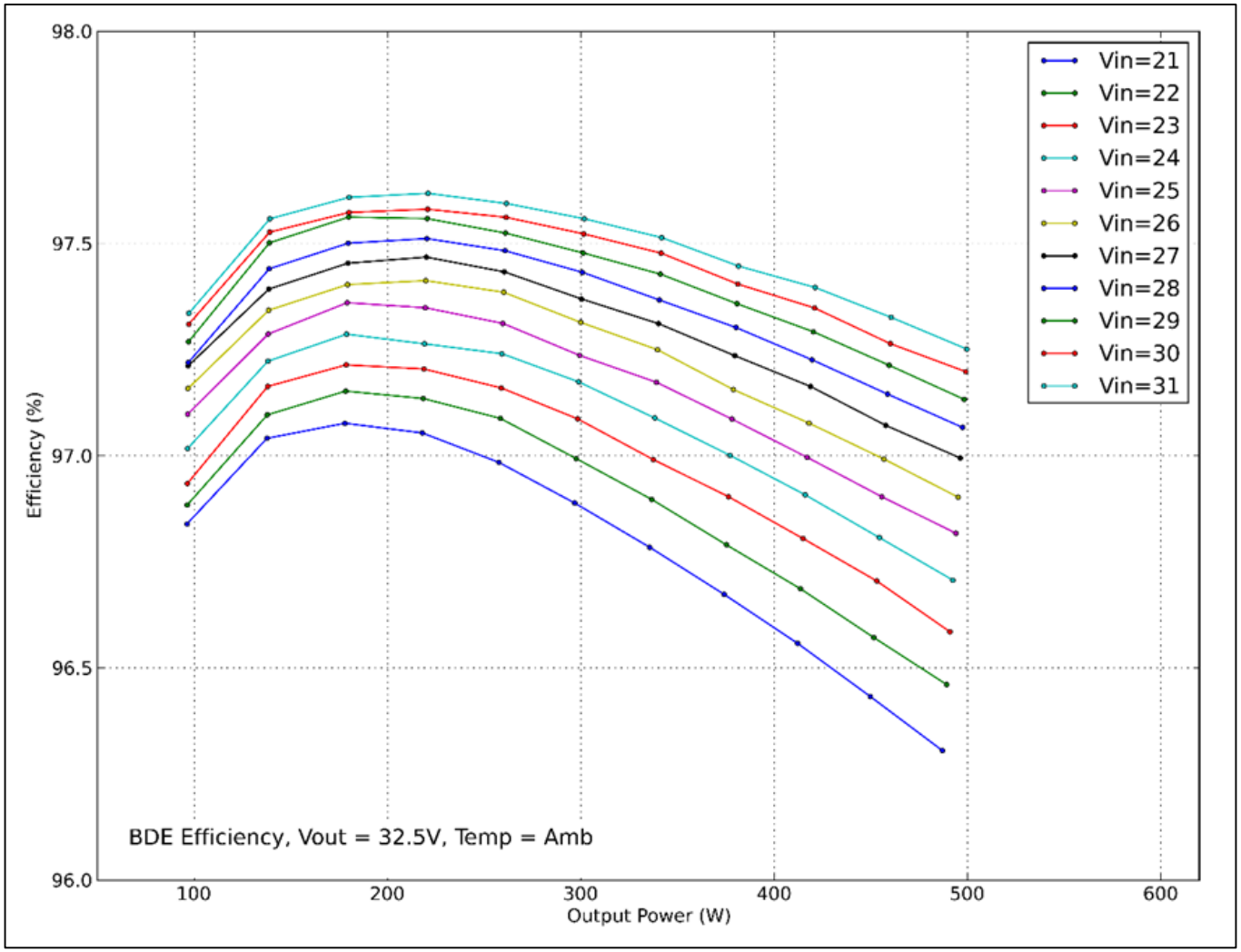
Better than expected: Very low overshoot on GaN FET Vgs and Vds waveforms

AEPS GaN Insertion: Breadboard Results (SSE)



An example of the detailed efficiency sweeps performed (Buck pwr stage)

AEPS GaN Insertion: Breadboard Results (BDE)



An example of the detailed efficiency sweeps performed (Boost pwr stage)

AEPS GaN Insertion: Breadboard Efficiency Comparison to Heritage Silicon Designs

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SSE (Buck)

Operating Point			Efficiency (%)		
Vin(V)	Vout(V)	Pout(W)	GaN	Si	Delta
45	32.5	300	98.2	97.6	0.6
		500	97.8	97.4	0.4
	28	300	97.5	96.9	0.6
		500	97.1	96.6	0.5
	25	300	97.0	96.4	0.6
		500	96.4	95.9	0.5
85	32.5	300	96.1	95.2	0.9
		500	95.8	95.4	0.4
	28	300	95.4	94.6	0.8
		500	94.9	94.6	0.3
	25	300	94.7	94.0	0.7
		500	94.1	93.9	0.2
			AVG		0.5

SSE avg efficiency improvement (%)
This is approx. 11% avg Pdiss reduction

BDE (Boost)

Operating Point			Efficiency (%)		
Vin(V)	Vout(V)	Pout(W)	GaN	Si	Delta
31	32.5	300	97.6	96.9	0.7
		500	97.3	96.5	0.8
28	32.5	300	97.4	96.6	0.8
		500	97.0	96.1	0.9
24	32.5	300	97.2	96.1	1.1
		500	96.7	95.4	1.3
21	32.5	300	96.9	95.6	1.3
		500	96.3	94.6	1.7
				AVG	1.1

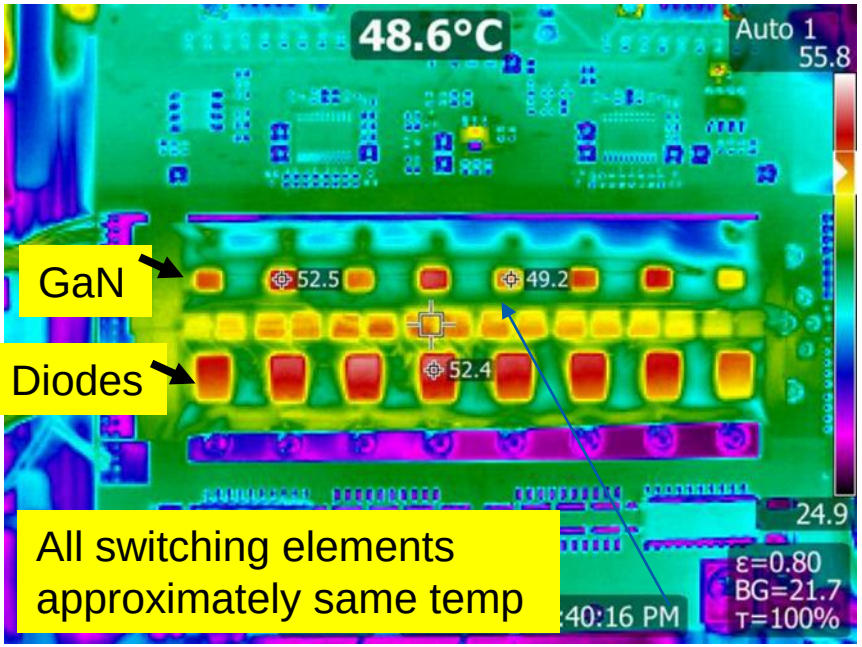
BDE avg efficiency improvement (%)
This is approx. 25% Pdiss reduction
(partially from FET voltage change)

Comparison between GaN breadboard and heritage design indicates efficiency improvement with new GaN boards, across all operating points, against a heritage design that was already highly optimized for efficiency

Caveats: This is a design before/after comparison, but it is not a pure Si/GaN device comparison due to other changes made concurrently

AEPS GaN Insertion: Breadboard Thermography

GaN Breadboard: SSE
Ambient air environment ~22C
Vin = 65V, Vout = 26.5V, Pout = 500W



Well balanced thermally

AEPS GaN Insertion: Conclusions

- The AEPS GaN breadboard effort successfully completed the goals of reducing board layout risk, showing part temperatures are acceptable via preliminary thermography, demonstrating improved manufacturability, and demonstrating increased efficiency

- **Next Steps:**
  - Build and test brassboard slices (including all PWM and control circuitry)
  - Get more direct “slice level” efficiency comparisons
  - Get parts approved for program use

Progressing through next steps towards adoption in flight designs

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