THE AEROSPACE CORPORATION

# Magnetic Saturation, A Lesson Learned from Battery Charger Power Electronics

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# Tentative Schedule of the Lesson-Learned Presentation

- For 2019 SPW:
  - *General overall description of  a power system with magnetic saturation*
  - *Top-level modeling concept for magnetic saturation*
  - *Consequential design improvements after the identified magnetic saturation*
- For 2020 SPW:  Modeling of Magnetic Saturation
  - *Modeling approach and detailed implementation for circuit simulation.*
- For 2021 SPW:
  - *Cause and Effect Relationship between Pulse-Skipping and Magnetic Saturation*

# Outline of the Lesson Learned

- Summary of Problem and a Flight Electrical Power System
- Aerospace Independent Analysis
- Battery Charger Test and Troubleshooting
- Battery Charger Modifications
- Summary of Aerospace Contributions

# Summary of Problem and Key Aerospace Contributions

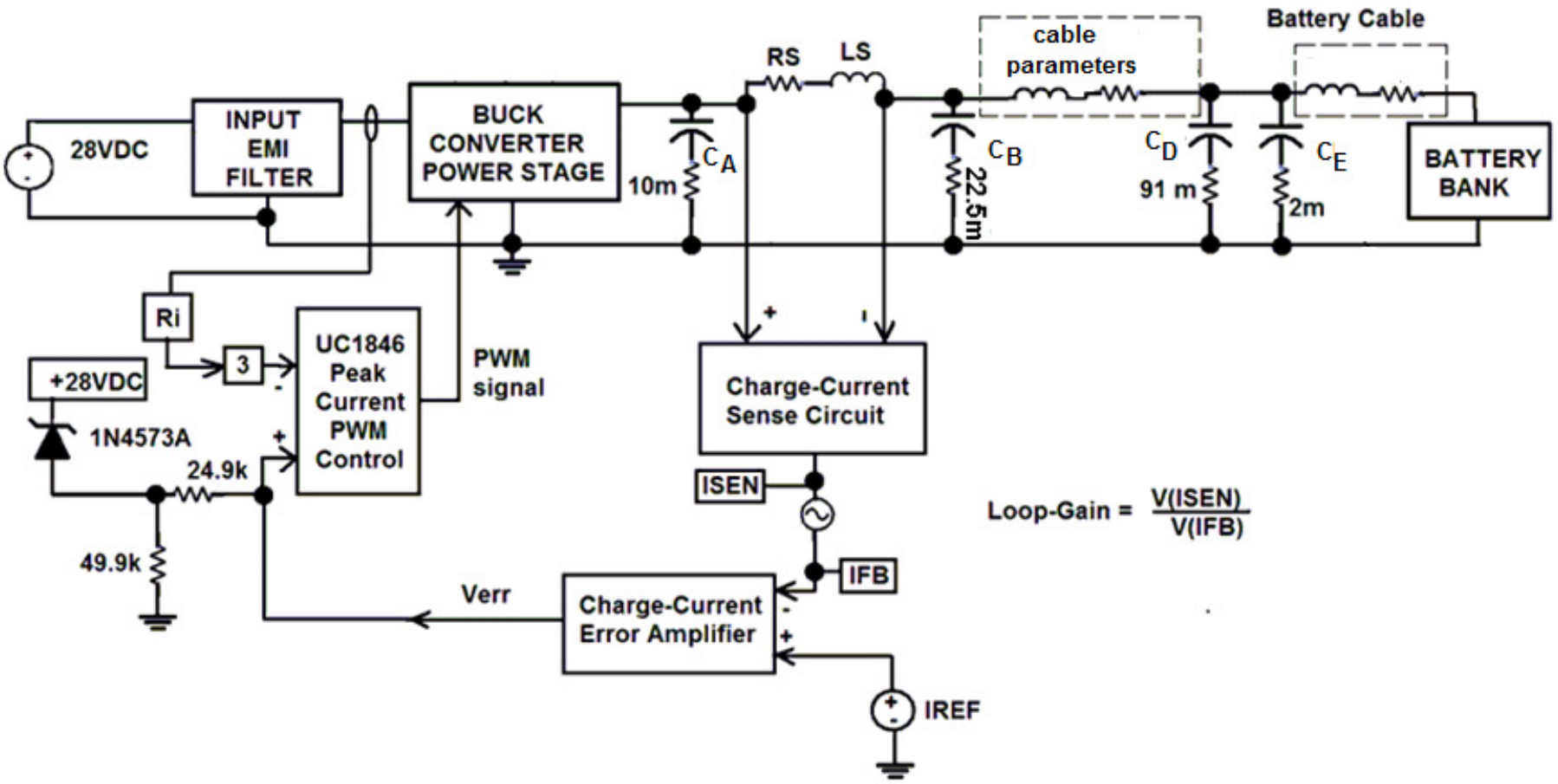
- The flight battery charger had a design flaw resulting in a charge current oscillation
  - *Generic flaw with a severe risk, up to loss of vehicle battery charging capability*

- Battery charge current noise, first observed during testing of a space vehicle (SV) by contractor, was the first symptom of an underlying issue
  - *Battery current telemetry varied instead of being at a steady charging current (12 A DC).*

- Aerospace's analysis uncovered a problem key to understanding the battery current noise, months before it was verified by test
  - *Circuit model included an effect absent from contractor's simulation: magnetic saturation*
  - *Simulation incorporating magnetic saturation showed a potential battery current oscillation*
  - *In response, the contractor thoroughly re-evaluated the battery charger design*
    - Leading to a removal of the battery charger hardware from the SV for inspection,
    - The inspection uncovered component overstress in the EMI filter as a result of the oscillation associated with the magnetic saturation.

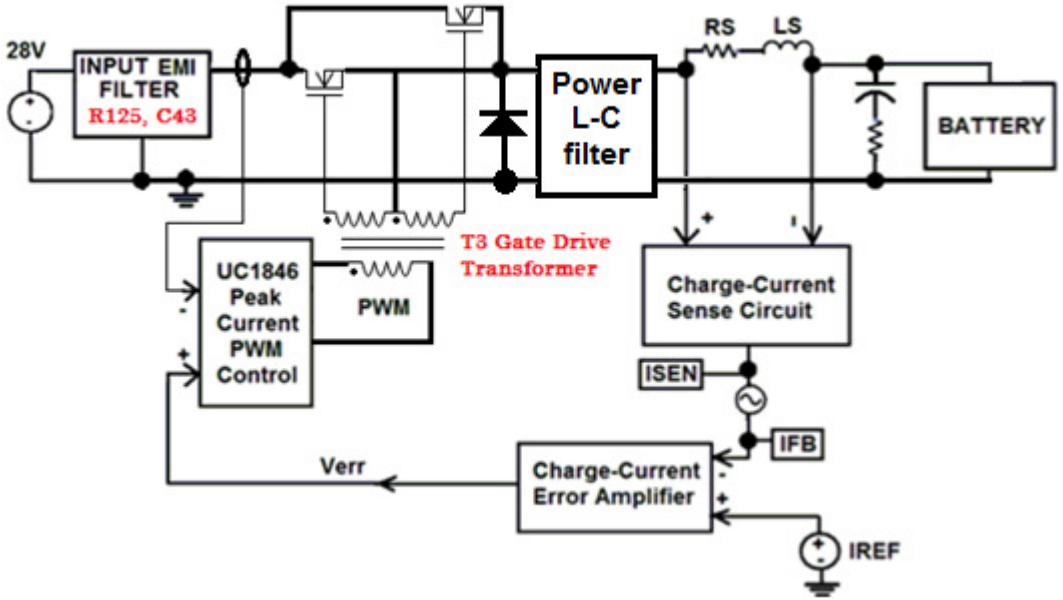
- Aerospace participated in root cause testing and the battery charger modification effort
  - *Implemented improvements to the root cause test setup and captured root cause waveforms*
  - *Suggested design upgrades and corrected problems with initial modifications*
  - *Corrected late-breaking issues with the modifications*

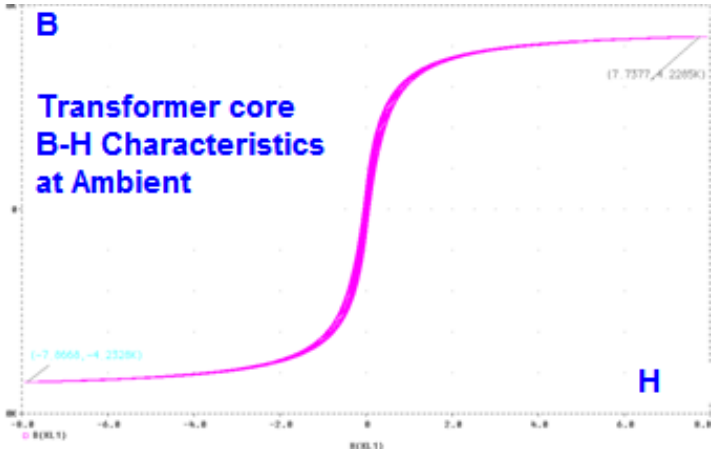
# Conceptual Diagram of Battery Charger Control Loop



# Identifying Magnetic Saturation as a Threat

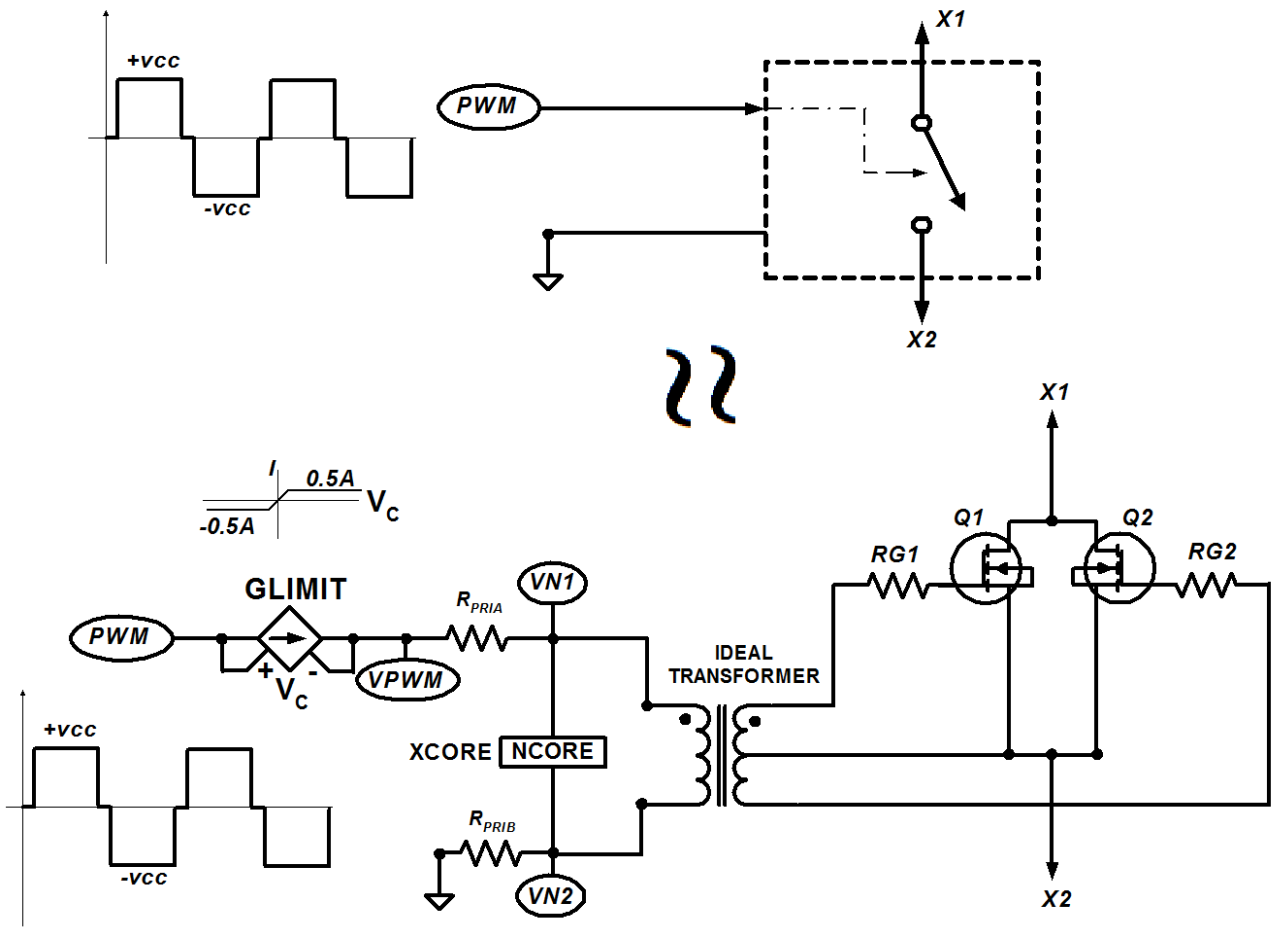
- Each battery charger contains a gate-drive transformer that communicates PWM control signals to the main MOSFETs
- This push-pull transformer lacked a mechanism to resist magnetic flux walking
  - *Residual DC voltage appeared across the primary (no capacitive blocking)*
- A sub-harmonic oscillation initiated magnetic flux walking by making the on-time of one phase longer than the other
- Magnetic saturation leads to loss of normal closed-loop battery charge current control
  - *Battery current oscillates at a frequency range from 100 Hz to 5 kHz of oscillation*
  - *The contractors verified and accepted this Aerospace finding*



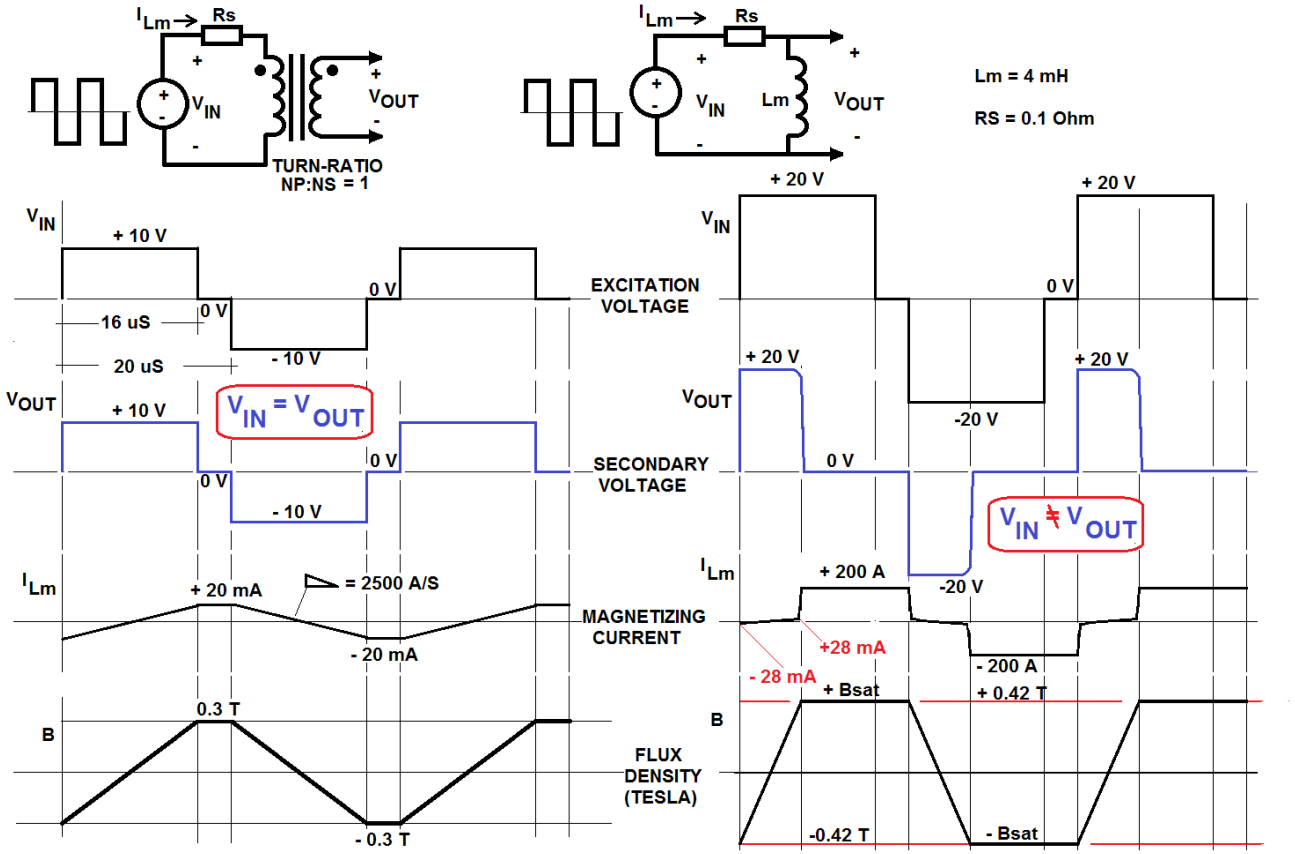

PWM: Pulse Width Modulator, MOSFET: Metal Oxide Field Effect Transistor

# Top-Level Modeling Diagram of PWM Switch with Saturable Transformer




- Saturable pulse transformer is decomposed into a non-linear device NCORE and an ideal transformer

# Conceptual Transformer Output Responses Without Magnetic Saturation VS with Magnetic Saturation




- Typical response of transformer output voltage without magnetic saturation (waveforms on the left) and that with magnetic saturation (on the right)

# Three Possible Levels of Magnetic Saturation

(1) Benign saturation:

- *Occurs at lower core temperature and its effect is unobservable (no truncation of pulse-width of transformer output voltage)*

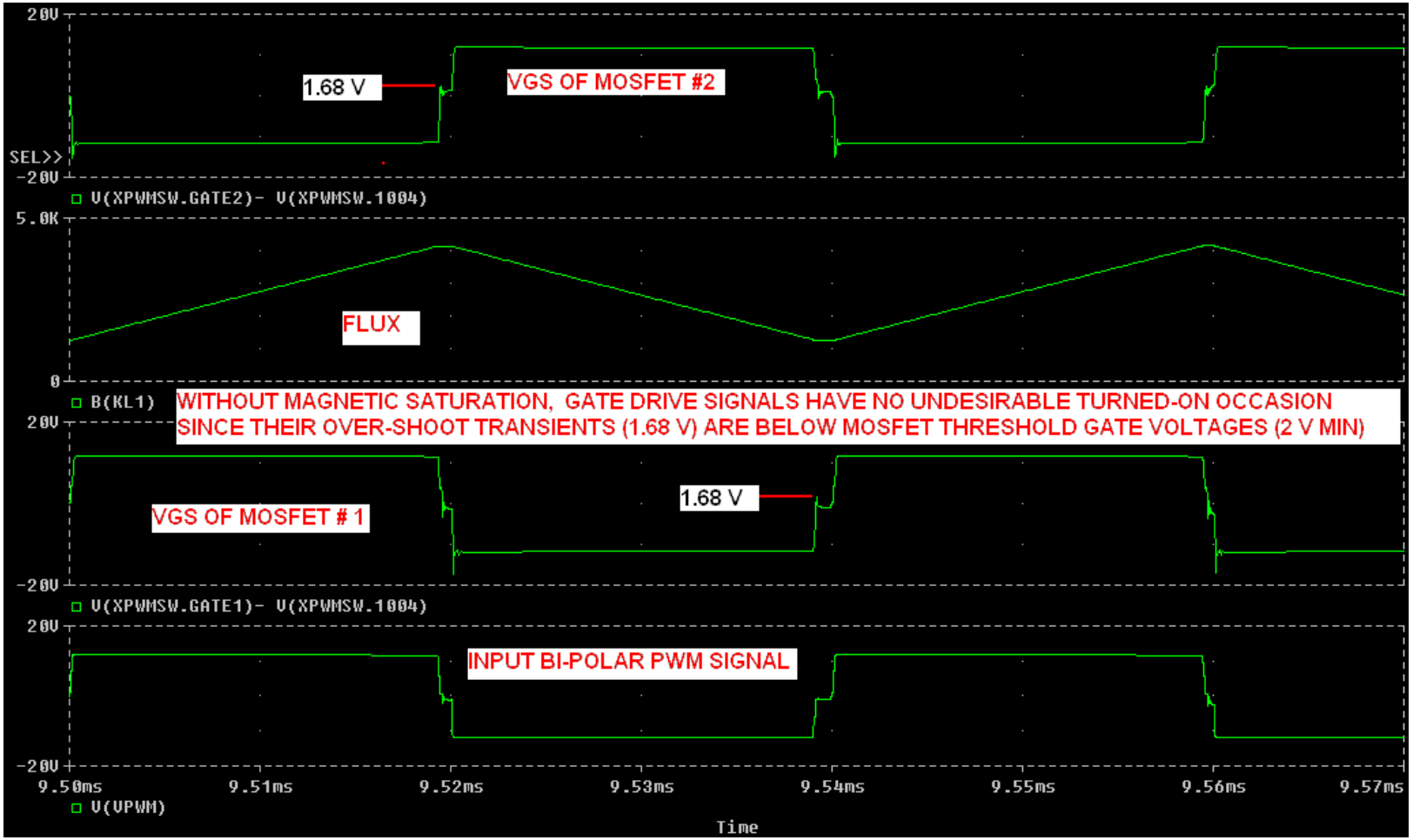
(2) Medium saturation:

- *Occurs at medium core temperature and its effect is observable with sporadic negative spikes in battery charge current (sporadic truncation of PWM pulse)*

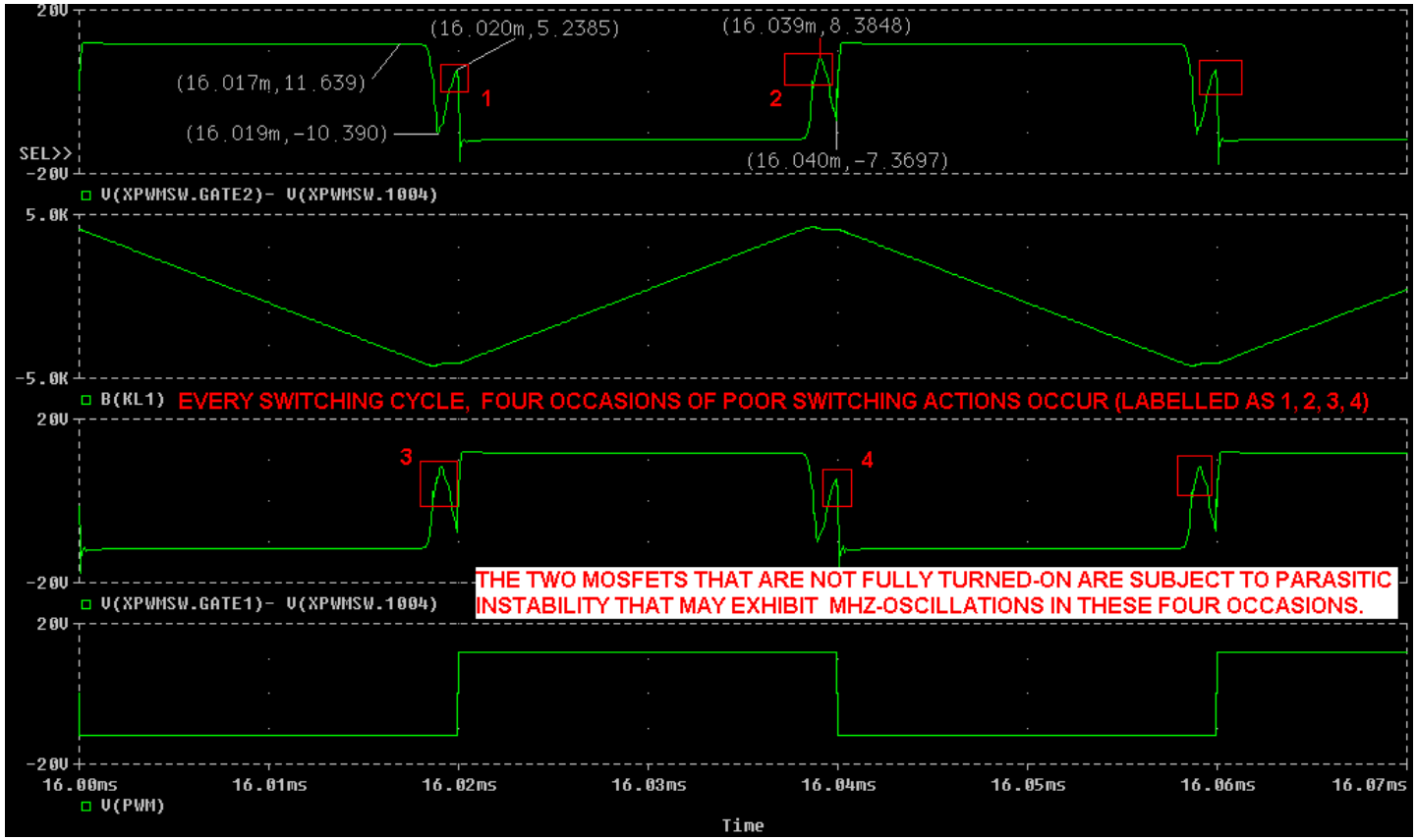
(3) Deep saturation:

- *Occurs at high core temperature and its effect is observable with charge current significantly dropped below its target charge rate (12 A) (truncation of PWM pulse at fundamental switching frequency), leading to a complete open-loop operation, i.e. the closed-loop PWM chip driver operating at a perfect square-wave driving voltage across the transformer primary winding.*

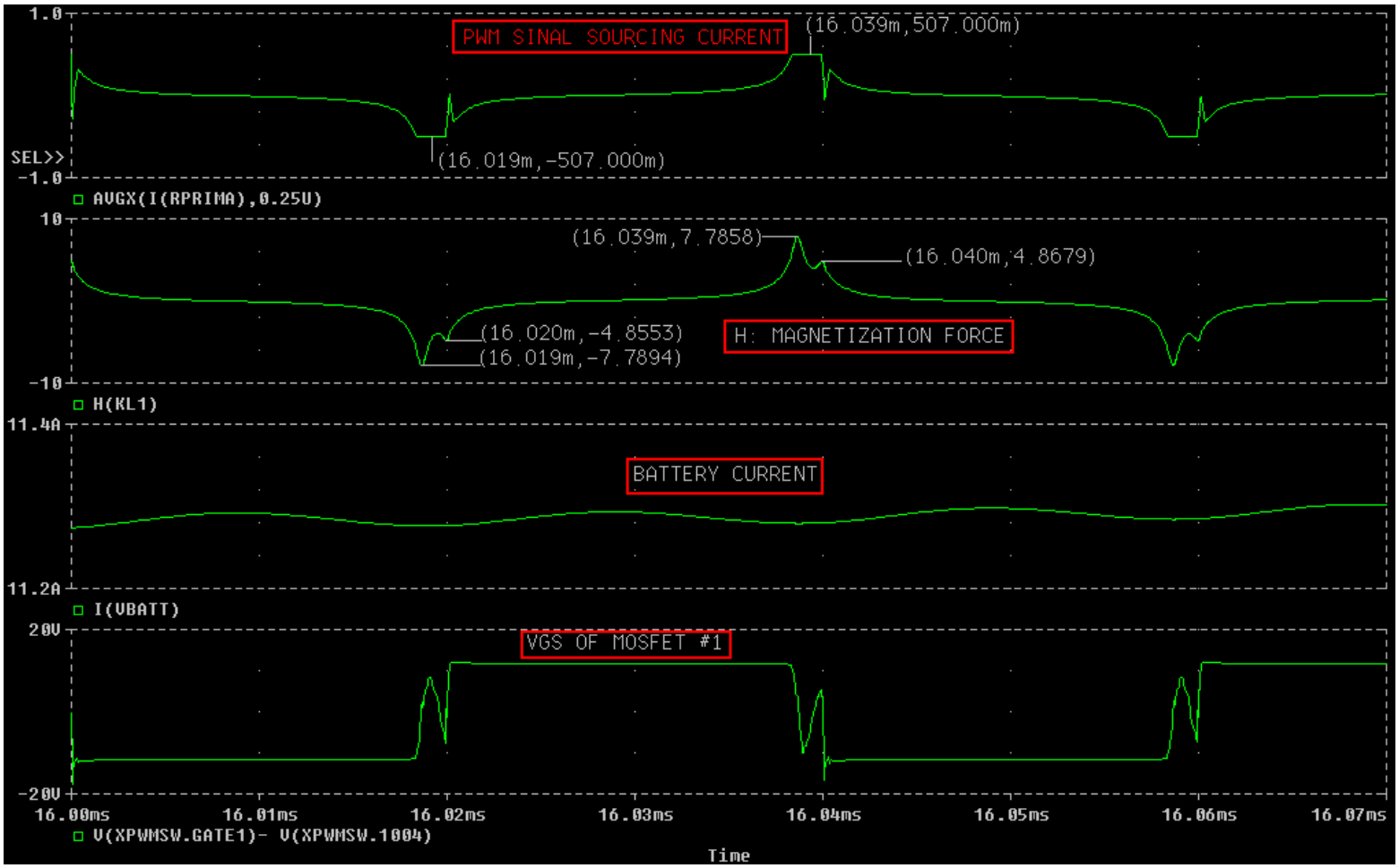
# Gate-Drive Signal from Benign Magnetic Saturation (or No saturation)



# Gate-Drive Signal from Pulse Transformer with Deep Magnetic Saturation

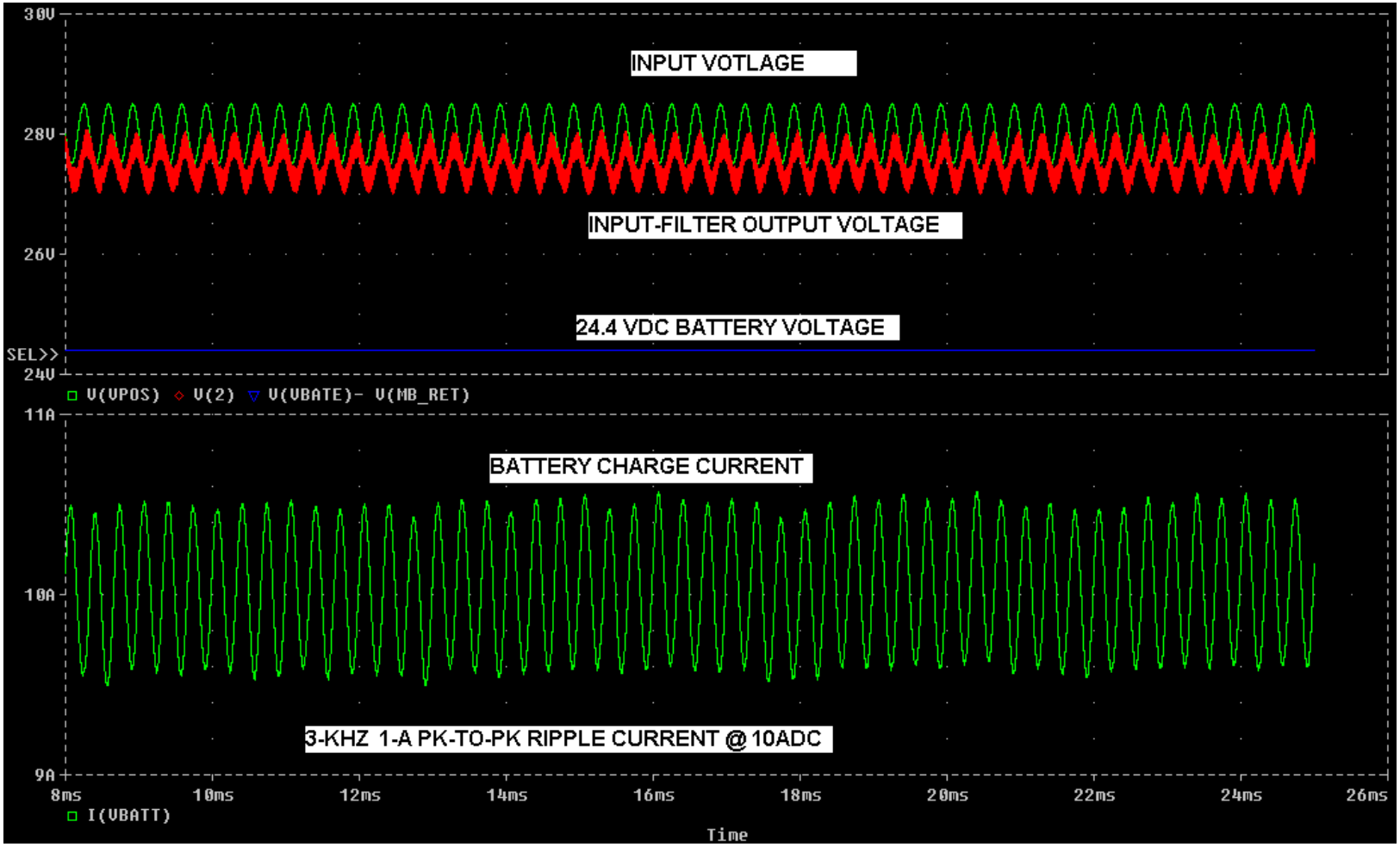


# Gate-Drive Signal from Pulse Transformer with Deep Magnetic Saturation (continued)



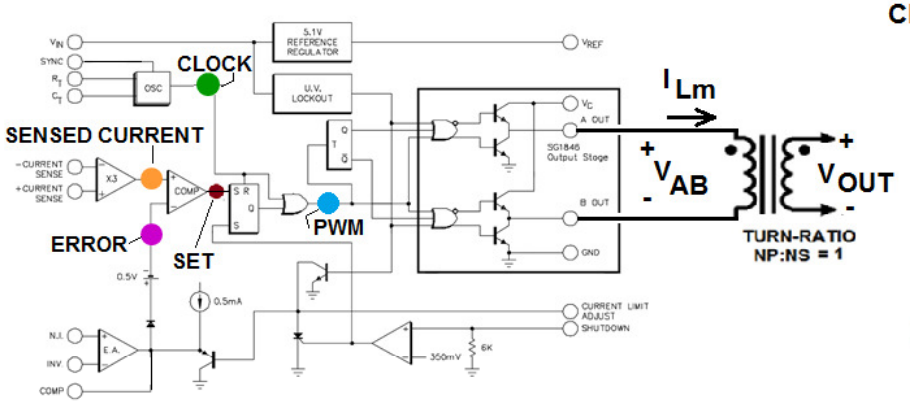
# End Result of Deep Magnetic Saturation

# Charger Control Loop Oscillation

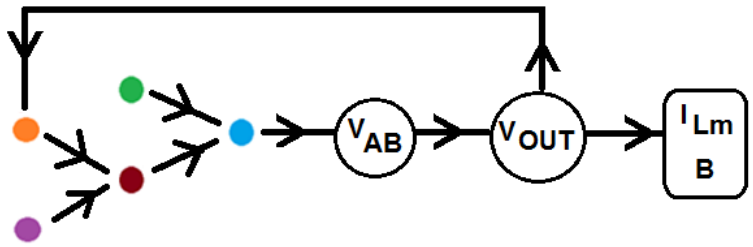


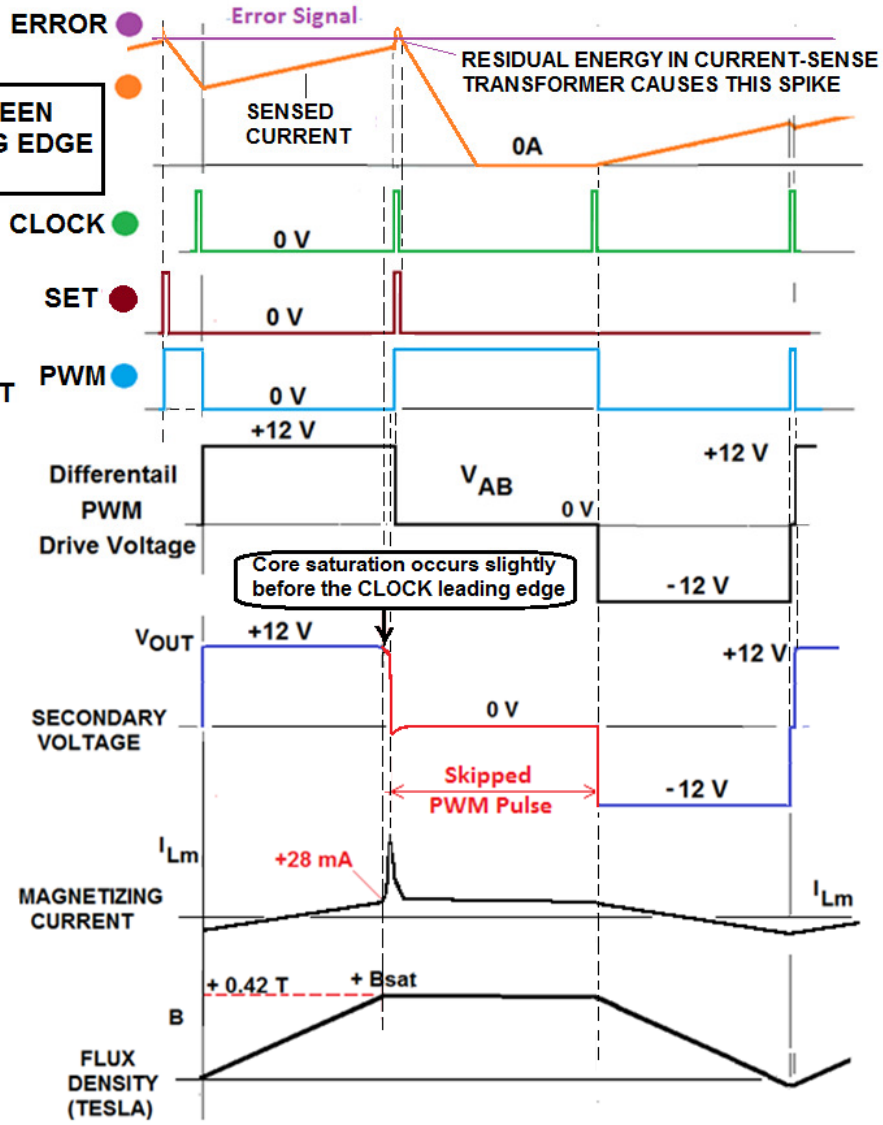
# Visualizing Magnetic Saturation and Pulse-Skipping

**PULSE SKIPPING OCCURS WHENEVER THE OVERLAPPING BETWEEN "CLOCK" ● AND "SET" ● SIGNALS REVEALS THAT SET'S FALLING EDGE HAPPENS AFTER CLOCK'S FALLING EDGE.**

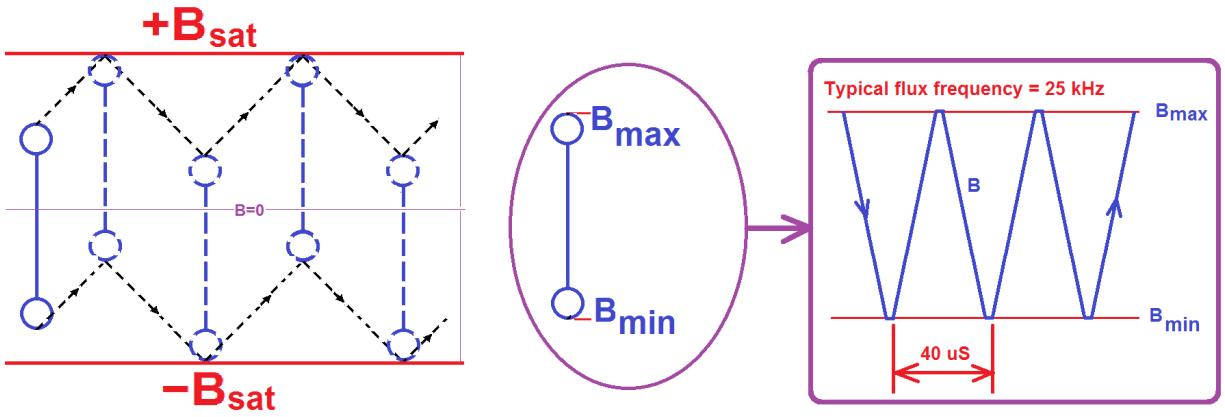



**Cause-and-Effect Diagram for Key Voltage and Current Signals**



# Magnetic Flux Walking in a Gate Drive Transformer

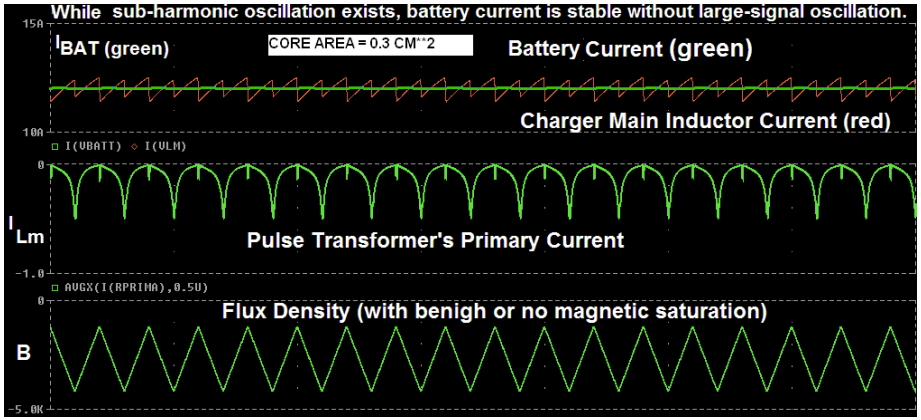



PING-PONG BEHAVIOR OF MAGNETIC FLUX IN PULSE TRANSFORMER

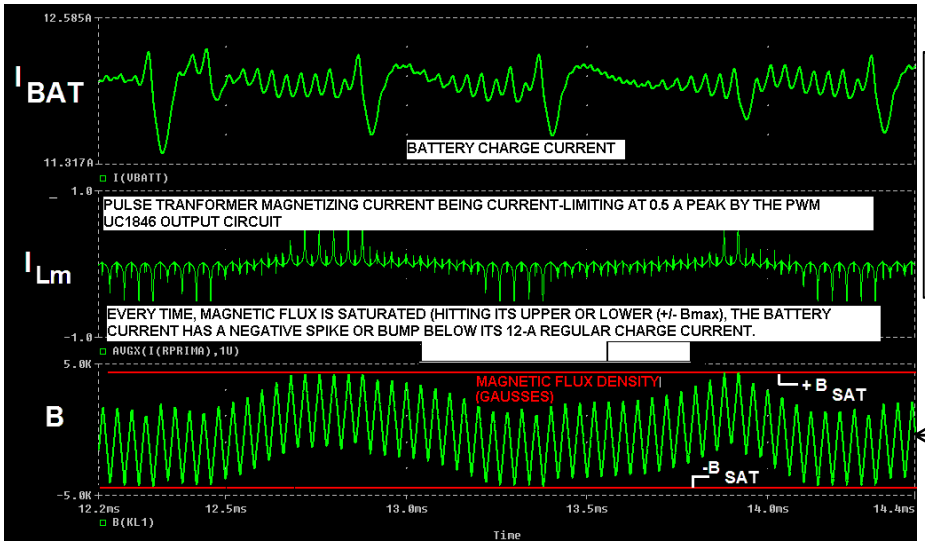
- One of three possible signatures of Magnetic Ping-Pong (**MPP**) waveform
- As **MPP** hits its saturation limit, either $+B_{sat}$ or $-B_{sat}$ , the saturation terminates ON-state of the charger switch and does not trigger pulse-skipping if the saturation happens in far proximity of the subsequent CLOCK pulse.
- Whenever the saturation happens in close proximity or overlaps with the PWM CLOCK pulse, the saturation will trigger pulse-skipping.

# Including Magnetic Saturation Predicts Oscillation

## Simulation with Magnetic Saturation Included




The upper plot shows the stable battery current whenever magnetic saturation is soft (verge of saturation or no saturation) . While sub-harmonics oscillation at 25 kHz exists, the battery current is not only stable but also has no large-signal ripple current (very flat @ 12 A with small AC ripple @ 50 kHz).




The lower plot shows how the battery current has negative bumps whenever magnetic saturation (flux response B hitting +/-$B_{SAT}$) is able to cause a significantly shorter turn-on pulse to the charger switch (without Pulse-Skipping).

Simulated flux walking between +$B_{sat}$ and -$B_{sat}$

# Effect of the Resulting Battery Current Oscillation

- The battery current oscillation had severe consequences for battery charger operation and reliability

1. *Component overstress, potentially leading to loss of the battery charger cards*

   a) Excessive power dissipation in the input filter damping resistor (9W vs. 1W rating), leading to loss of the resistor and an even larger battery current oscillation
   b) Ripple current overstress in the input filter's wet-slug tantalum capacitor
      i. Under such a condition, hermetically sealed wet slug capacitors fail catastrophically
      ii. Such a failure would introduce FOD into the critical battery charger
   c) Excessive power dissipation in the PWM controller chip

2. *Performance impacts*
   a) Loss of normal closed loop battery current control
   b) High bus ripple current and battery ripple current
   c) Degraded efficiency

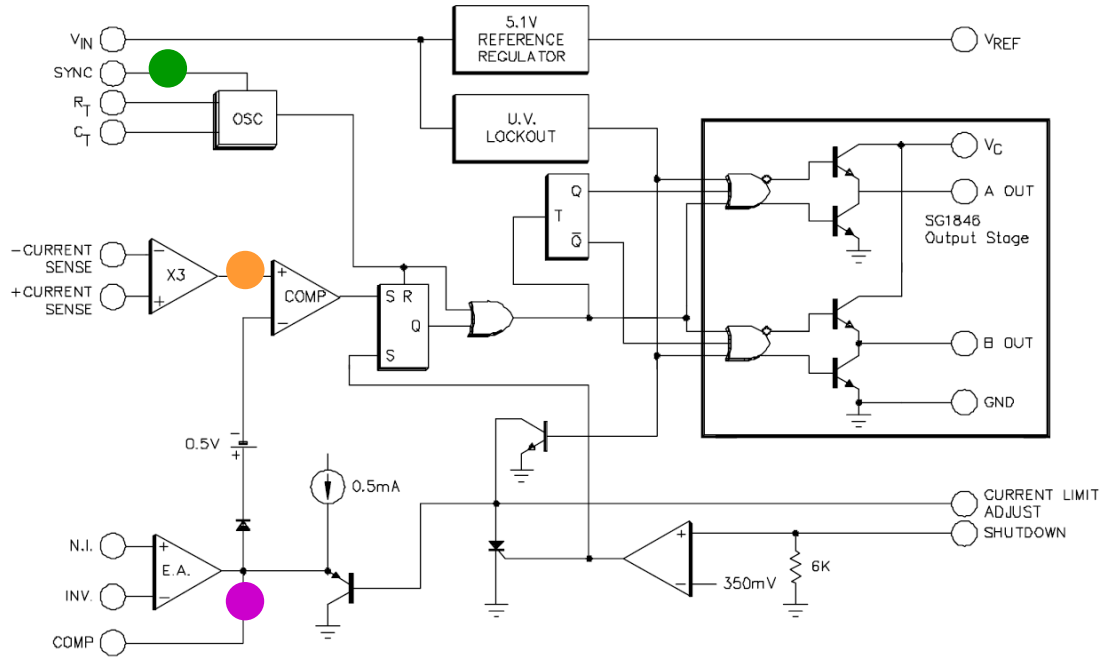
3. Mission Impacts: Thermally run-away to the PWM controller chip and the saturated Transformer

   a) Insufficient battery charging current during sunlight in eclipse season, or
   b) Complete battery charger failure (stop charging the batteries during sunlight)

FOD: Foreign Object Debris

# Root Cause Data for Battery Current Dropouts

**PWM Chip Schematic**



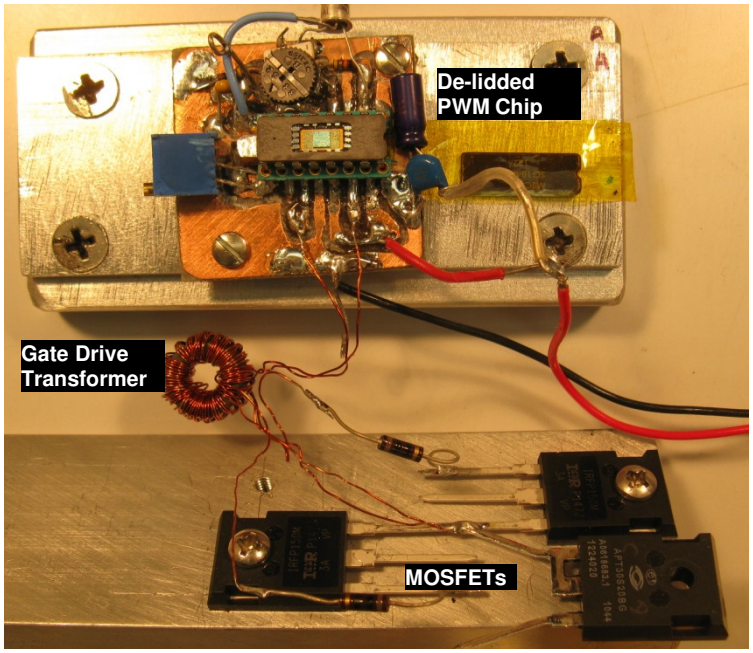

- Key signal timing difference: current sense (orange) remains above the error voltage (purple) during the clock (green, dead time)
  - *Main MOSFET does not shutoff within the dead time*
  - *Results in PWM chip simultaneous "set" and "reset" condition*
  - *For this "undefined" SR latch condition, both outputs stay low*

- Signature reproduced in the EPSD lab using simple breadboard

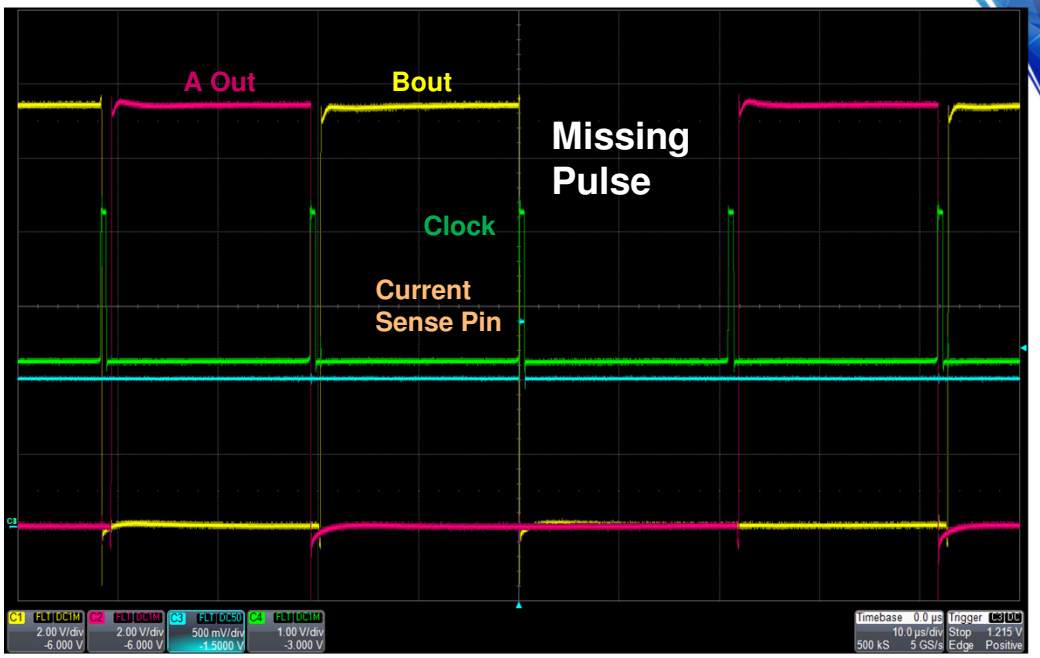
SR Latch: Set Reset Latch

# EPSD Breadboard Test Demonstrated Root Cause

**EDL Breadboard**




**EDL Breadboard Reproduced Failure Signature**




- Reproduced PWM chip upset signature in the EPSD lab
  - *Forced current sense pin high during the clock pulse*
  - *Both PWM outputs (red, yellow) stayed low, replicating the previous test data taken at the sub-contractor location.*

- Breadboard also used for PWM chip thermal characterization in the Parts Lab

EPSD: Electronics and Power Systems Department, EDL: Electronics Development Lab

# Battery Charger Modifications and Verification

- Modifications ensured that switching cycle terminates before the clock pulse

- Contributors to the timing problem
  - *High charge current extends switching cycle into the PWM chip dead-time*
  - *Sub-harmonic charge current oscillation causes gate drive transformer core walking*
  - *Pulse transformer saturates, causing loss of  PWM chip authority over MOSFETs*

- Mitigate or eliminate contributors:
  - *Improve timing margin*
    - Lower the DC charge current from 12A to 8A
    - Increase PWM chip dead-time
  - *Increase slope compensation to eliminate sub-harmonic oscillation*
  - *Change gate drive transformer core to a material with 3x higher saturation flux density*
  - *Clamp voltage spikes that were outside PWM chip ratings*

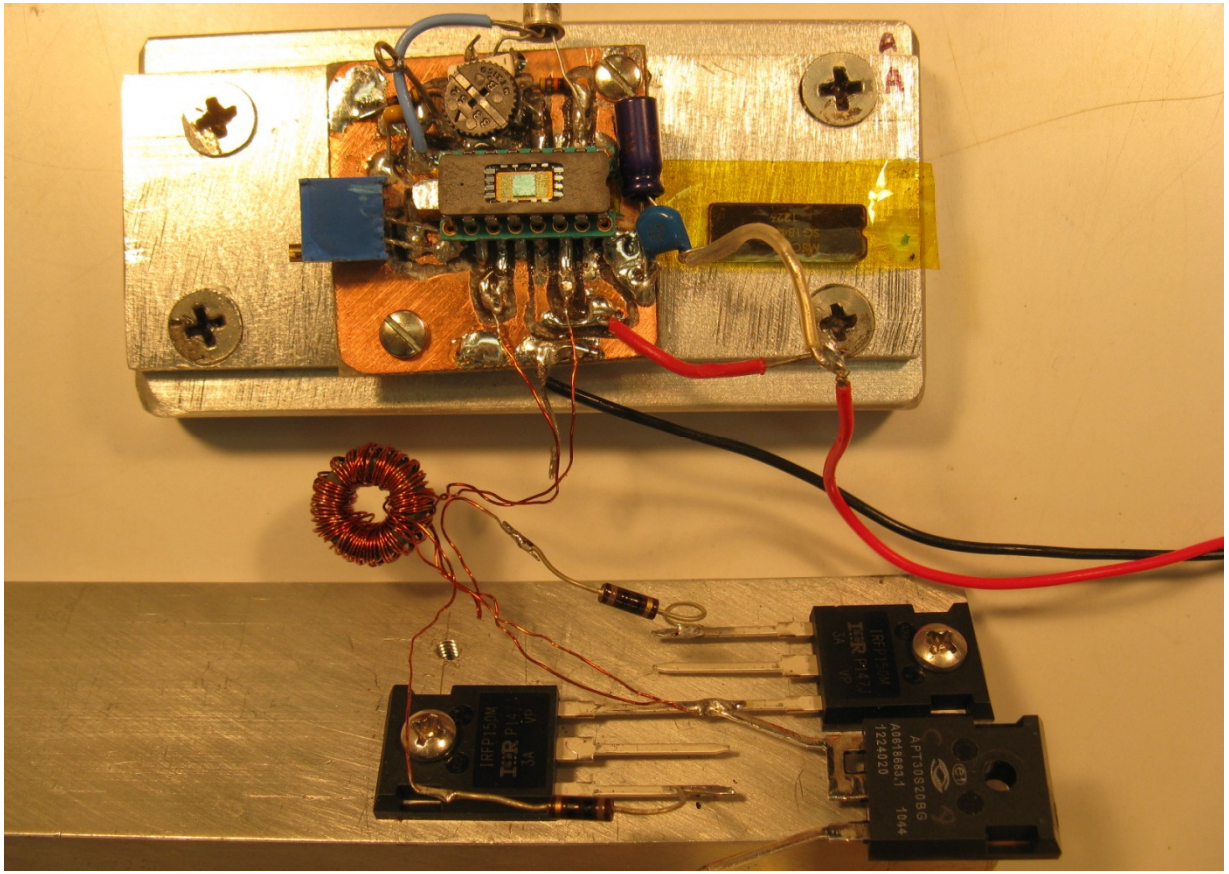
- Contractor implemented and verified the design upgrades within a year later
  - *Used the engineering unit of the battery charger to verify the upgrades.*

# Backup

# Aerospace Independent Verification of Charger Modifications

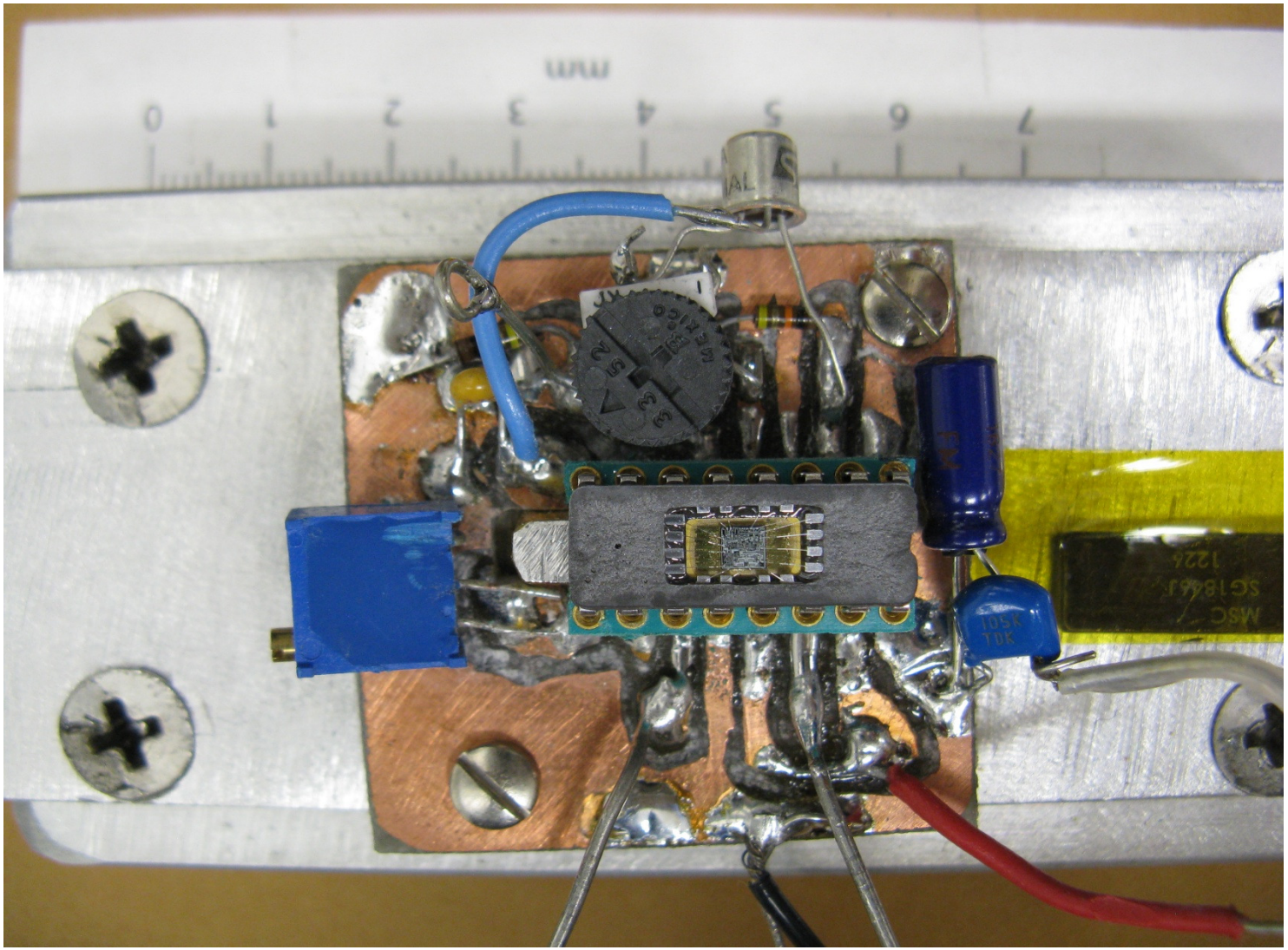
| Performance Item | Before Redesign | After Redesign |
|---|---|---|
| Regular Charge Current | Based Line Value = $I_{CHG}$ | Reduced to = $I_{CHG}$ - 4A |
| Bus Voltage Regulation<br>In Charge Reduction Mode | Low Phase margin (PM)<br>@ a reduced charge current | +20 degrees > the BR PM<br>(BR = Before Redesign) |
| Bus Voltage Regulation<br>In Shunt or Boost Mode | Acceptable Phase and Gain Margins | Unchanged |
| Charge Current Regulation | Healthy Phase Margin | +13 degrees > the BR PM |
| V/T Control Mode<br>@ 20 V Battery Voltage | Healthy Phase Margin | + 18 degrees > the BR PM |
| Charger Short-Circuit Current | Limited to ~ 2.6*$I_{CHG}$ | Limited to 2.5*$I_{CHG}$ |
| Pulse-by-Pulse Current Limiting | 1.25*$I_{CHG}$ @ 25 V Battery Voltage | 1.46*$I_{CHG}$ @ 25 V Battery Voltage |
| Pulse Transformer<br>Saturation Flux Density (Gausses) | 3300 G @ Hot Temp | 12000 G @ Hot Temp<br>(change core material) |
| PWM Dead Time | 2.5% of Charger Switching Period<br>(Presence of Pulse-Skipping) | 5% of Charger Switching Period<br>(Eliminate Pulse-Skipping) |
| If Battery Bus filter Capacitors<br>were open-circuit | Unstable Charge Current Regulation<br>(oscillation or instability) | Still Stable Charge Current Regulation<br>(Healthy PM ) |

# EDL Working Breadboard of Charger PWM and Switches



- This simple breadboard was constructed to find the conditions for output pulse-skipping
- The trimpots were adjusted to simulate precursor modes of operation found during ABQ testing
- The gate drive transformer was hand-wound using a purchased core to drive the buck MOSfets
- The De-lidded IC in this photo was also used for thermal imaging

# PWM IC De-lidded Configuration for Thermal Imaging



# PSPICE NETLIST CODE FOR PWM SWITCH WITHOUT DRIVING TRANSFORMER

```
.SUBCKT PWMSW ACTIVE1  ACTIVE2 PASSIVE COMMON VS1  VS2 PARAMS: L=10U
*
* SWITCHING CELL USING PWM
*
*
HCCVSA  1100    0      VL1     1
RHCCVS  1100    0      100MEG
RG1     GATA1   GATE1    10
RG1B    GATE1   1004     1G
*RLM1    ACTIVE  ACTIV1   0.001
*LM1     ACTIVE  ACTIV1   26N
CDS1    ACTIVE1   1004     1500P
CDG1    ACTIVE1  GATE1    500P
M1      ACTIVE1  GATE1    1004  1004  IRF540
*
RG2     GATA2   GATE2    10
RG2B    GATE2   1004     1G
*RLM2    ACTIVE  ACTIV2   0.001
*LM2     ACTIVE  ACTIV2   26N
CDS2    ACTIVE2   1004    1500P
CDG2    ACTIVE2  GATE2    500P
M2      ACTIVE2  GATE2    1004  1004  IRF540
*
RXM1    VS1     VS1A   0.01
XM1     VS1A     VS2   GATA1   1004   DCXFMR PARAMS: N=1
RXM2    VS2     VS2A   0.01
XM2     VS2A     VS1   GATA2   1004   DCXFMR PARAMS: N=1
*SGPWM   ACTIVE  1004    (VS1,VS2)  SMOD
*SHPWM   ACTIVE  1004    (VS2,VS1)  SMOD
VPWM    1004    PASSIVE DC=0
L1      1004    1005    {L}
VL1     1005    COMMON  DC      0
.ENDS
.model IRF540        NMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0 Vmax=0 Xj=0
+                    Tox=100n Uo=600 Phi=.6 Rs=21.34m Kp=20.71u W=.94 L=2u Vto=3.136
+                    Rd=22.52m Rds=444.4K Cbd=2.408n Pb=.8 Mj=.5 Fc=.5 Cgso=1.153n
+                    Cgdo=445.7p Rg=5.557 Is=2.859p N=1 Tt=142n)
*                    Int'l Rectifier           pid=IRFC140          case=TO220
```

# PSPICE NETLIST CODE FOR “NCORE” Saturable Inductor Model

```
.PARAM  AL = 2505E-3
.PARAM  PI = 3.1415927
*.PARAM  BM = 12000
*.PARAM  BM = 4000
*.PARAM  BM=3500
.PARAM  BM=2850
*.PARAM  BM = 2500
.PARAM  AC=0.148
*.PARAM  AC=1.48
.PARAM BI=1P
.PARAM UO={4*PI*1E-7}
.PARAM LME = 3.12
.PARAM UR = {AL*LME/AC*(1E-4)/UO}
.PARAM SVSEC = {BM*AC*1E-8}
.PARAM IVSEC = {BI*AC*1E-8}
.PARAM N=26
.PARAM K=500
.PARAM LMAG = {(1E-2)*UO*UR*AC*N*N/LME}
.PARAM LSAT = {(1E-2)*UO*AC*N*N/LME}
.PARAM RSA  =  {LSAT*K/(2*SVSEC*N)}
.PARAM RLM  =  {LMAG*K/(2*SVSEC*N)}
.PARAM RLM2 =  {0.5*LMAG*K/(2*SVSEC*N)}
.PARAM RLMB =  {RLM2*RLM/(RLM - RLM2)}
*
```

```
*
* NON-LINEAR MAGNETIC MODEL WITHOUT HYSTERESIS
*
.SUBCKT  NCORE  N1  N2  GAUSS
*
G1  0    FUX  N1  N2  1
E1 FLUX  0  VALUE= {V(FUX)}
F1 N1      N2    VM   1
CB FUX   0   {2*SVSEC*N/K}  IC = {0.5*K*IVSEC/SVSEC}
VM FLUX              N12  DC=0
RB1 N12  0      {LMAG*K/(2*SVSEC*N)}
RS N12   N23  {LSAT*K/(2*SVSEC*N)}
DS2  N22   N23   DX
DS1  N23   N4    DX
R3    FUX   0       1G
VS2  N22   0  DC=-250
VS1  N4     0  DC=250
*
RB2   N12    N33  {RLMB}
DXS2  NX22   N33   DX
DXS1  N33    NX4    DX
VXS2  NX22     0  DC=-175
VXS1  NX4      0  DC=175
*
* COMPUTE FLUX DENSITY IN GAUSSES
*
EGUASS   GAUSS  0  VALUE={V(FLUX)*BM*2/K}
RGUASS   GAUSS  0   1G
.ENDS
.MODEL DX   D(IS=1E-15)
```