

Adiabatic Power (APOL) CMOS Controller ASICs Flight Insertion Status

THE VALUE OF PERFORMANCE.

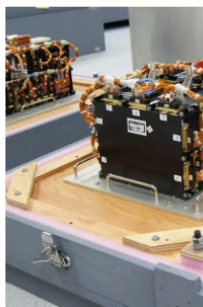
NORTHROP GRUMMAN

March 20, 2019

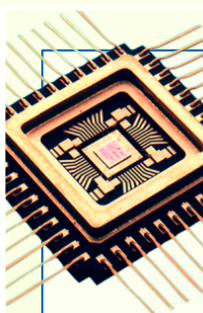
Henry Kuo, Dong Tan, Tim Hsia, and Henrik Gevorkyan



1. PwrCMOS ASICs: Key Feature



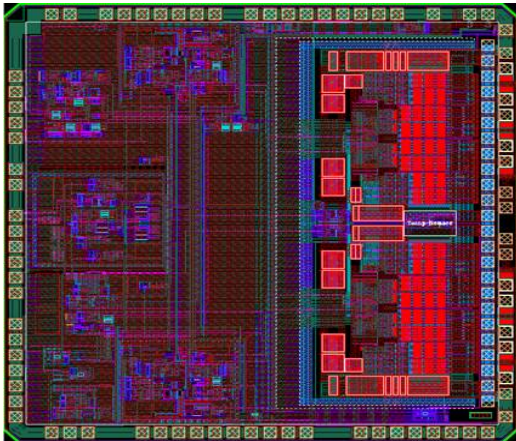
2. PwrCMOS ASICs: Key Performance



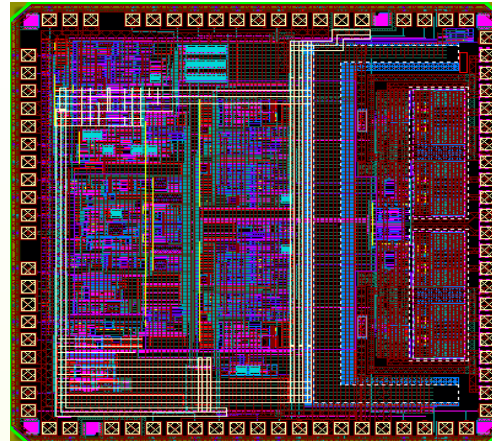
3. PwrCMOS ASICs: Radiation Test

- Custom mixed-signal power controller ASICs are a technological discriminator for NGAS' leading-edge power products
 - Components integration translates into improvements in power, size and mass, which in turn lead to cost savings
 - Customization creates flexibility for the development of end-to-end system architecture, requirements, and application-specific features

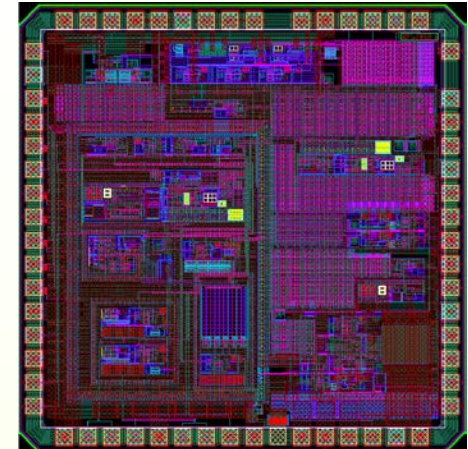
Power Controller ASICs: Overview



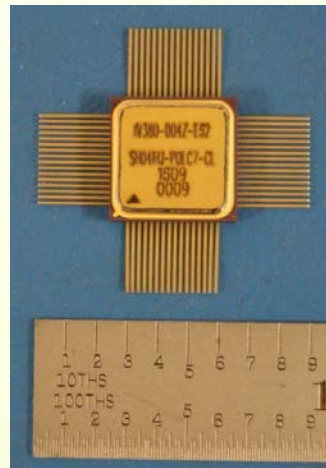
BCMP ASIC Die
4.2 mm x 4.2 mm



POLC ASIC Die
4.25 mm x 4.25 mm



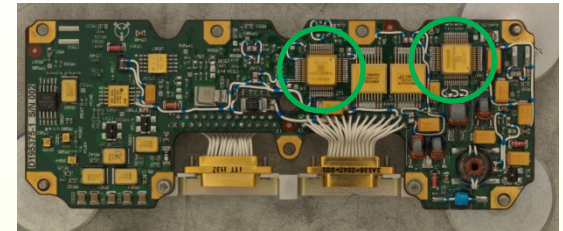
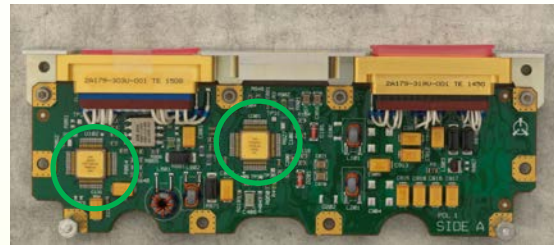
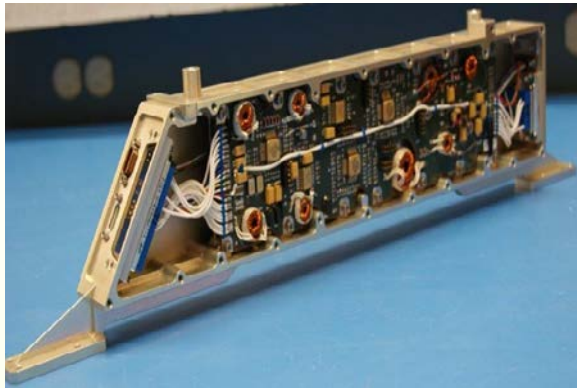
SF/LDO ASIC Die
2.83 mm x 2.83 mm



Key Features:

- Silicon foundry process: IBM 7HV 180nm Power CMOS technology
- Package: 64-pin CQFP
- Full-custom analog mixed-signal design from device (transistor) level and up

POLC and SF/LDO Application Examples

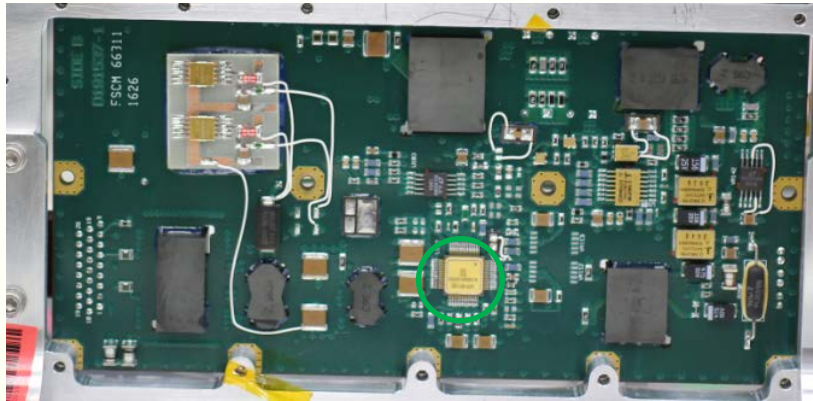


- Multi-channel outputs
 - Positive and negative
- Converter types:
 - Forward
 - Flyback
 - Buck
 - LDO
- Output power: ~20W
- Command/telemetry
- Primary-redundant unit
- Flight production in progress

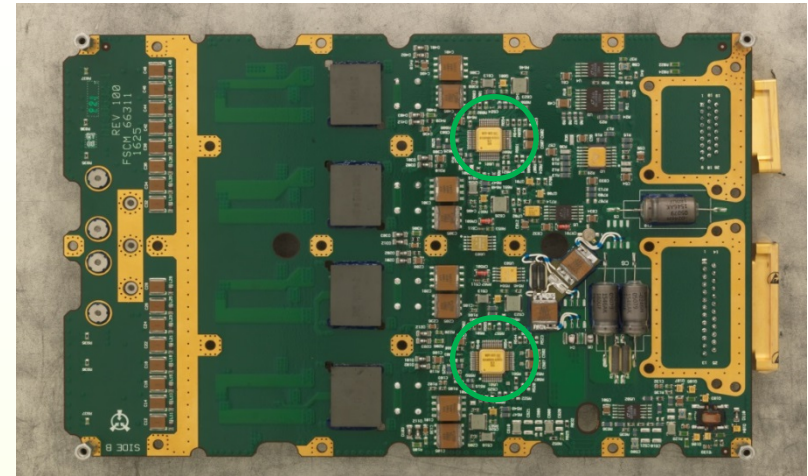
- Multi-channel outputs
- Converter type: Buck
- Fast dynamic response
- Tight DC regulation ($\pm 3\%$)
- Output power: ~10W
- Passive bi-level command/telemetry
- Flight production in progress

- Multi-channel outputs
 - Positive and negative
- Converter types:
 - Buck
 - Flyback
 - LDO
- Ultra low output ripple
- Flight production in progress

BCMP Application Examples



- Multi-channel outputs
 - Positive and negative
- Converter types:
 - Double-Forward
 - Flyback
- Output power: ~30W
- Sub-mV output ripple
- Sub-mV conducted susceptibility
- Primary-redundant unit
- EM in test



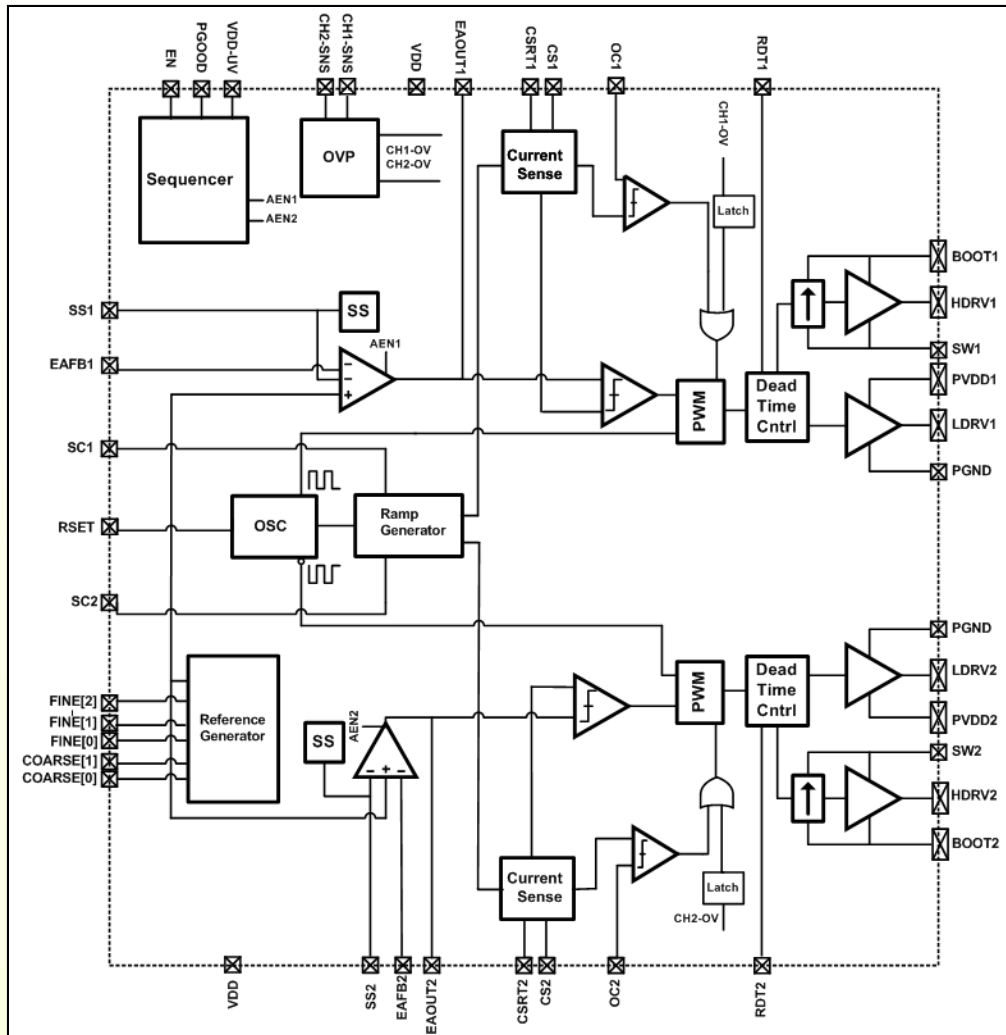
- Single outputs via 4-channel current sharing
- Converter type:
 - Double-Forward
- Output power: ~450W
- Provides bus isolation
- > 85% efficiency at EOL
- 4-channel synchronization performed by 2 BCMP controller ASICs
- EM in test

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1. PwrCMOS ASICs: POLC and SF/LDO

POLC ASIC Functional Block Diagram and Features

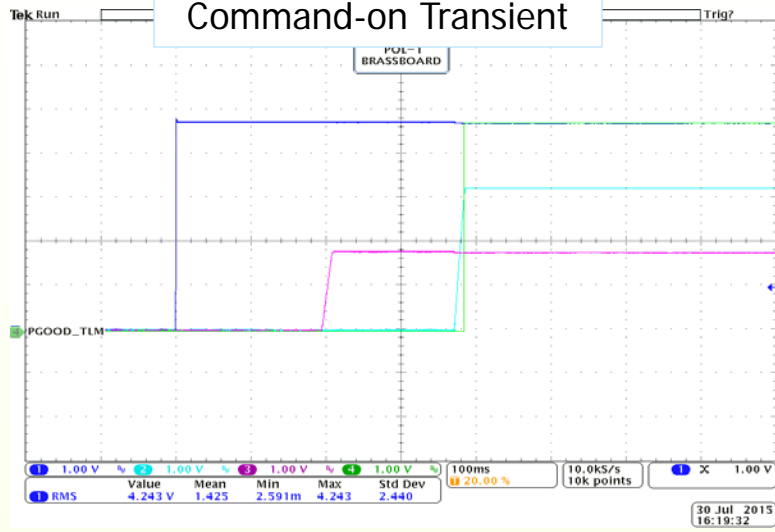


POLC ASIC Features

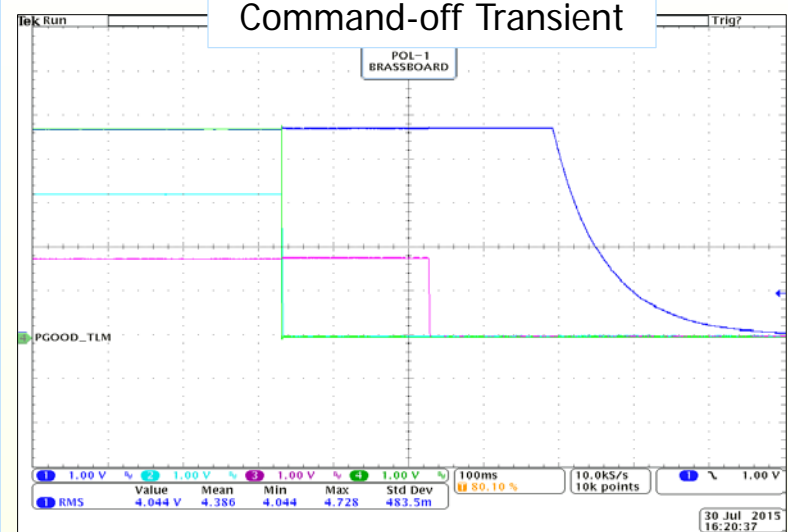
- Two independent interleaved PWM Current Mode controllers
- Programmable frequency up to 500kHz
- Dead-time control
- Over-current protection
- Slope compensation
- Integrated drivers with bootstrapped high-side driver
- Coarse and fine tuning of reference
- Programmable soft-start
- Programmable Input under-voltage lockout (UVLO)
- Over-voltage protection
- Active power sequencing

Hardware Test Results: POLC

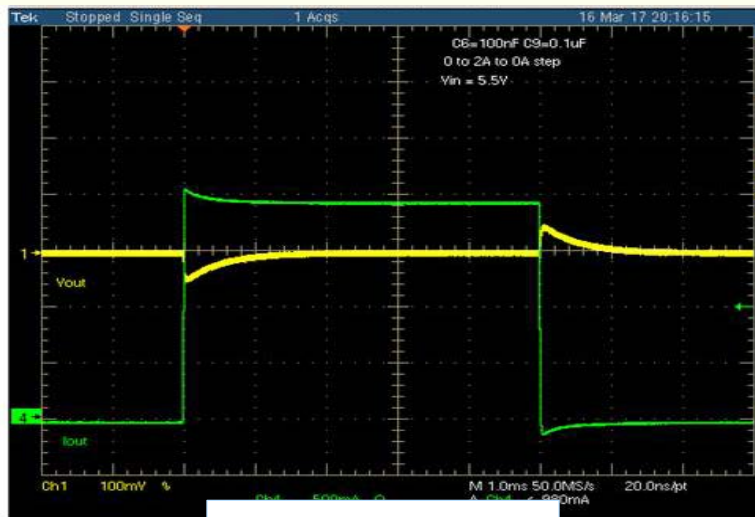
Command-on Transient



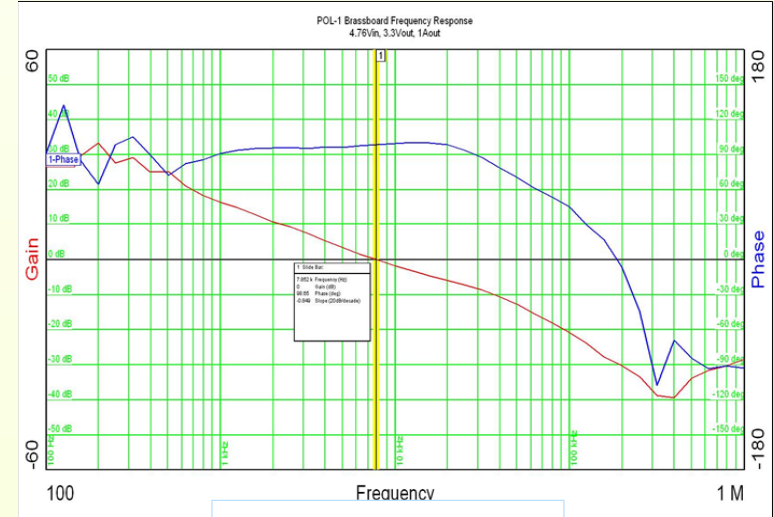
Command-off Transient



Step Load

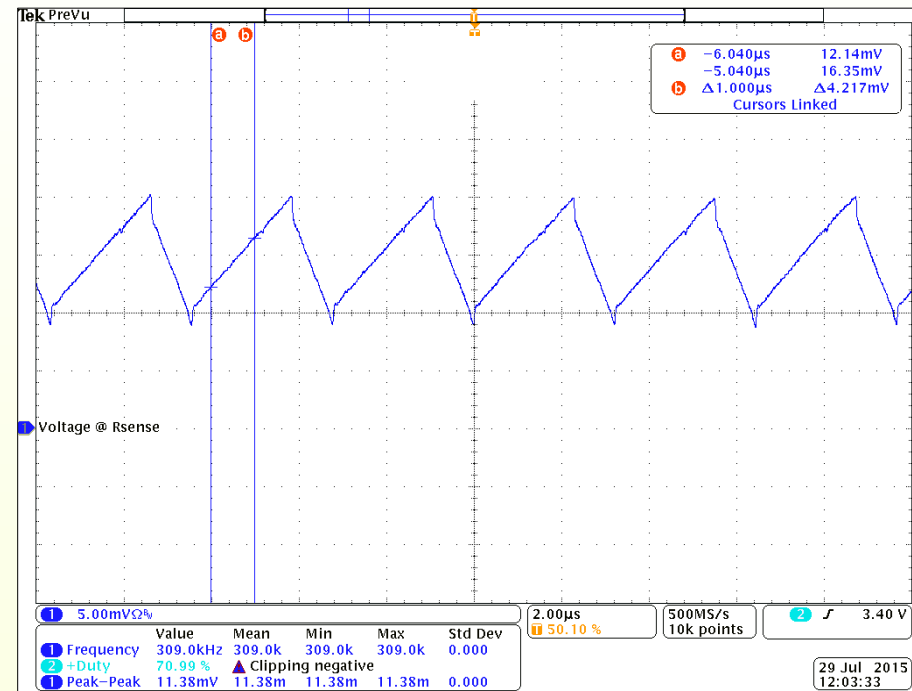
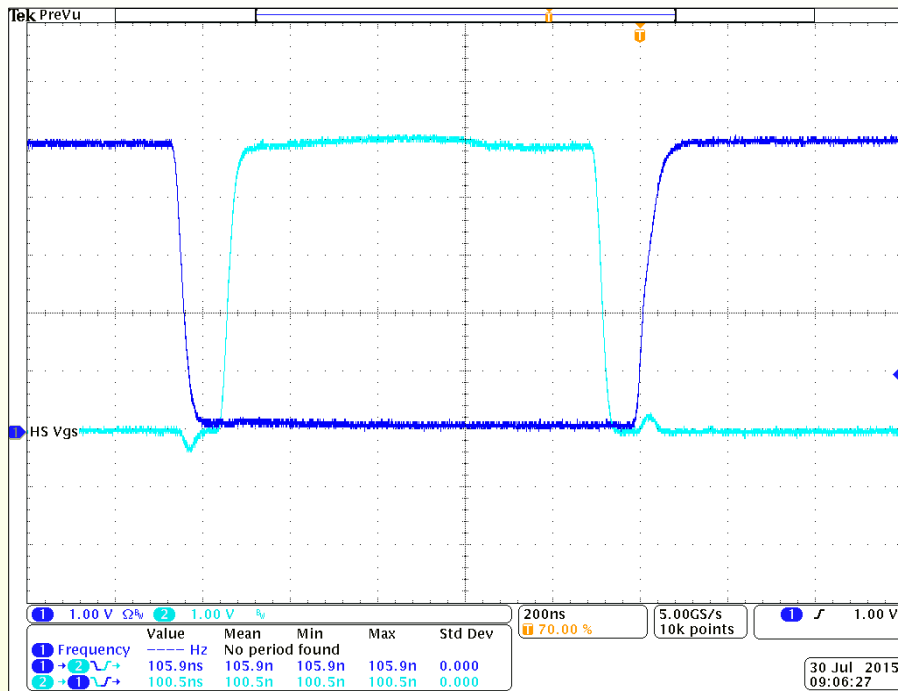


Loop



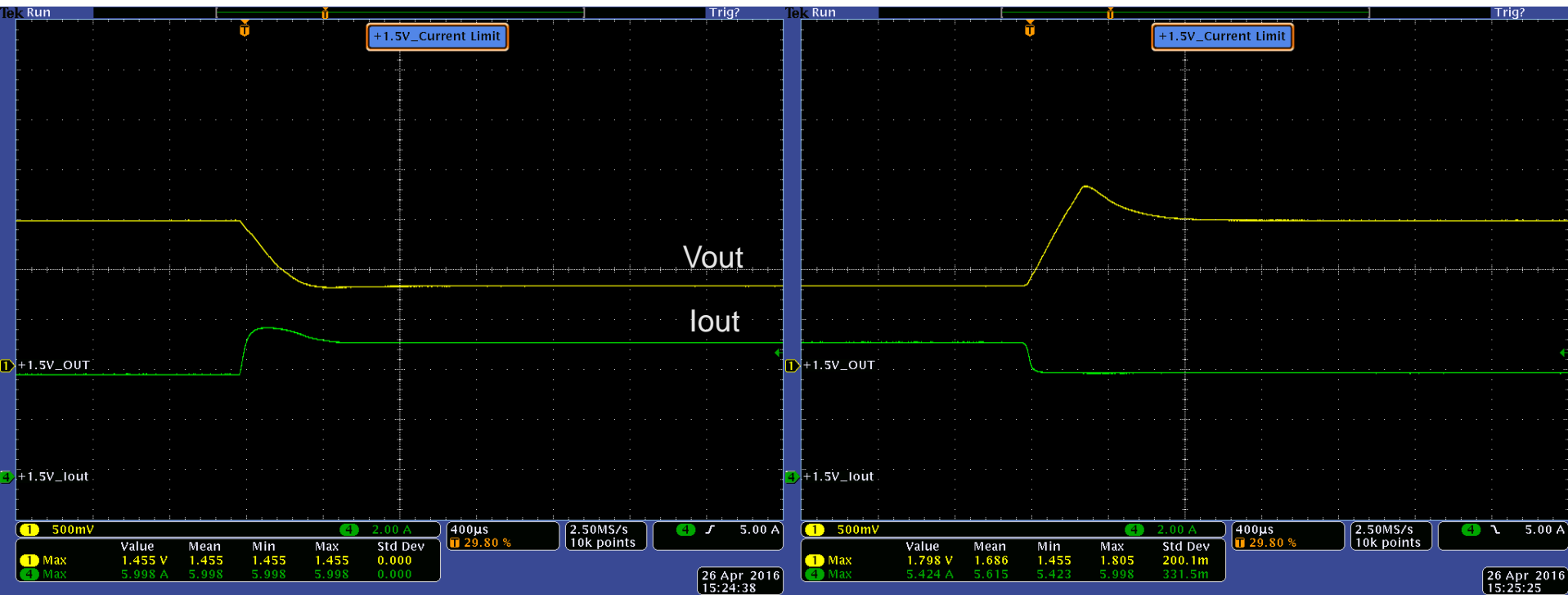
Hardware Test Results: POLC

- Gate drive signals & output inductor current waveforms



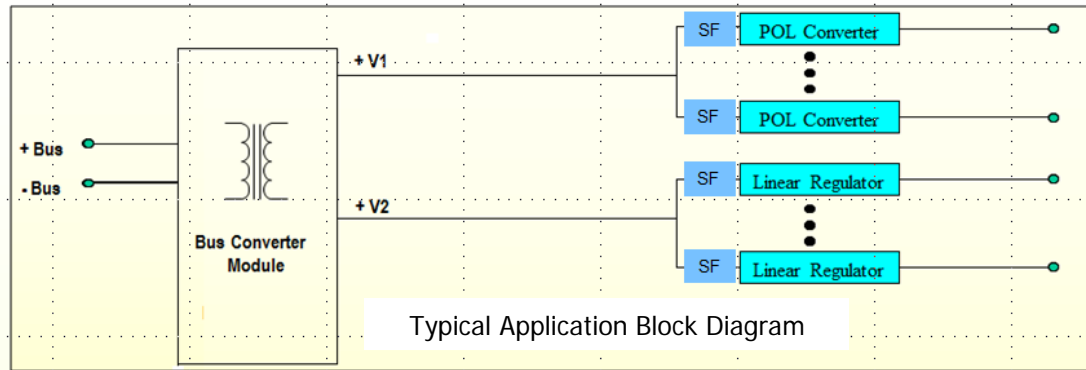
Clean waveforms indicate solid design

Peak Current Limit Simulation Waveforms: POLC

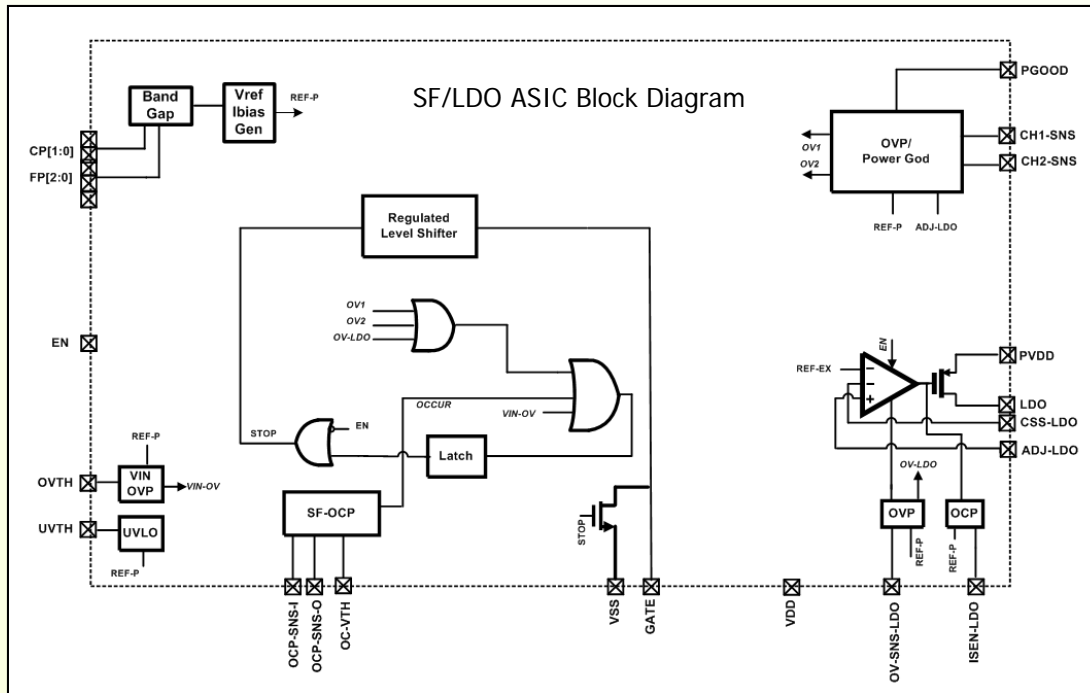


Peak current limiter is fully functional

SF/LDO Functional Block Diagram and Features



Typical Application Block Diagram

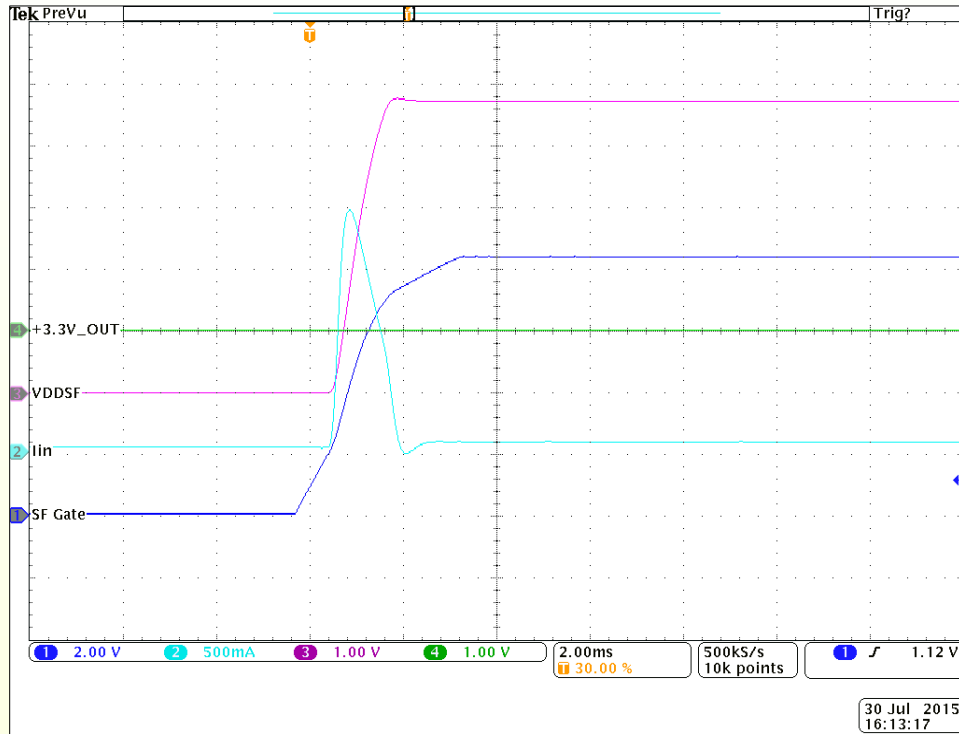


SF_LDO3 ASIC Features

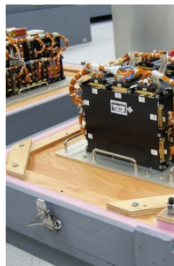
- Programmable Smart Fuse (SF) open threshold
- On-chip regulated level-shifter SF switch driver capable of driving high capacitive load
- Programmable input supply Under-Voltage-Lock-Out
- Programmable input supply over-voltage protection
- Integrated LDO with on-chip Power MOSFET with OCP/OVP
- Over-voltage protection sensing and logic circuitry for additional external output channels
- Power Good telemetry

Hardware Test Results: SF/LDO

- Smart fuse start-up waveform

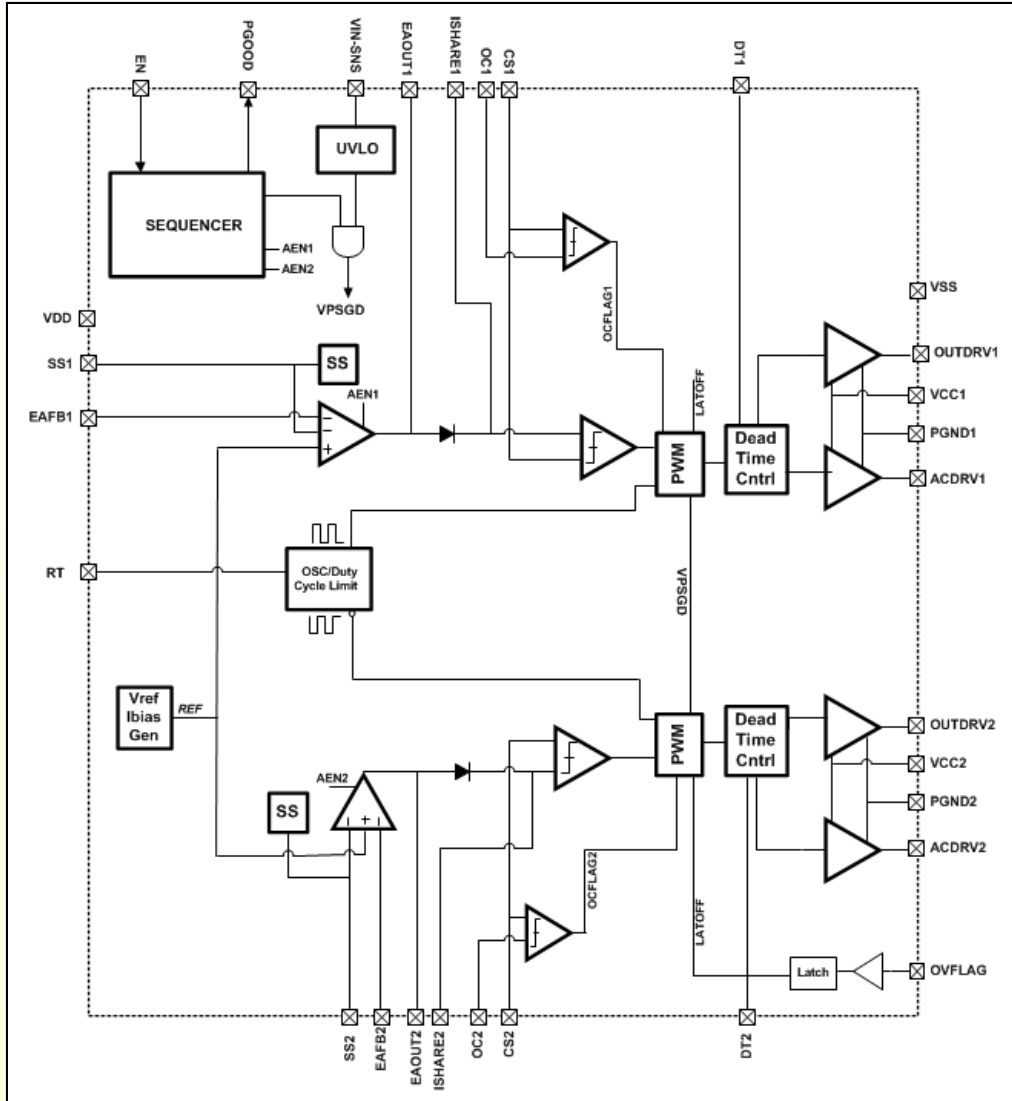


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2. PwrCMOS ASICs: BCMP

BCMP ASIC Functional Block Diagram and Features

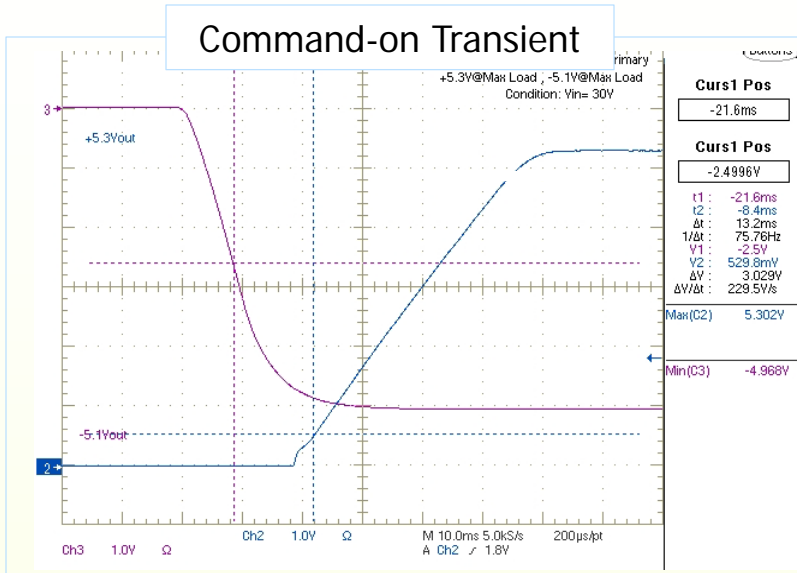


BCMP ASIC Features

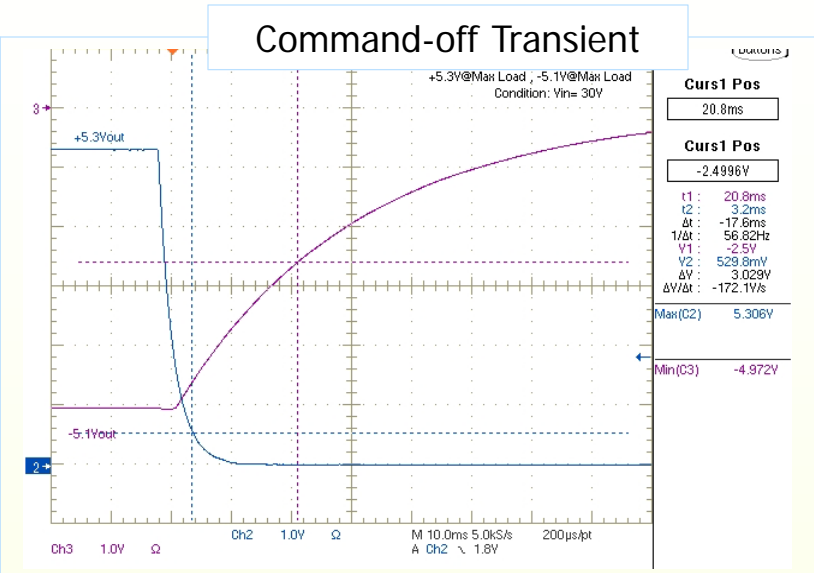
- Two independent interleaved current mode PWM controllers
- Current-sharing
- Programmable frequency up to 500KHz
- Over-current protection
- Integrated high-voltage drivers
- Programmable soft-start
- Programmable input Under-Voltage Lock-Out (UVLO)
- Over-voltage protection
- Active power sequencing
- Max duty cycle limiter
- Power good telemetry

Hardware Test Results: BCMP

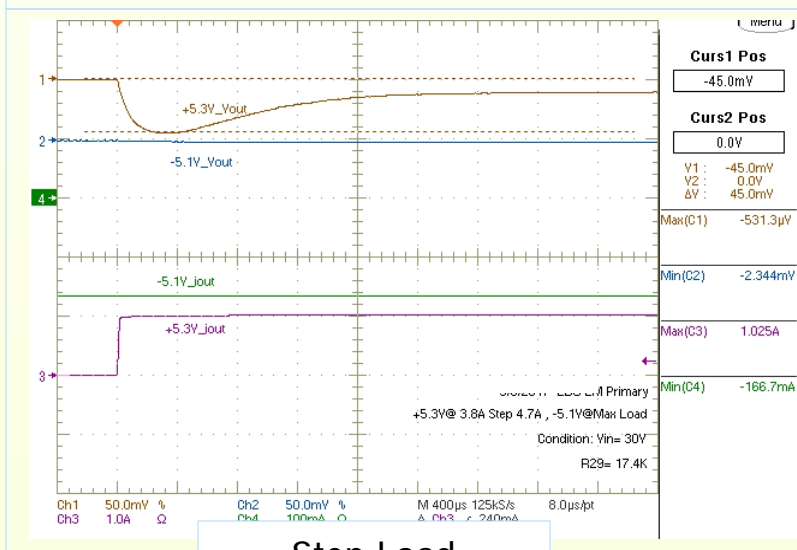
Command-on Transient



Command-off Transient



Step Load

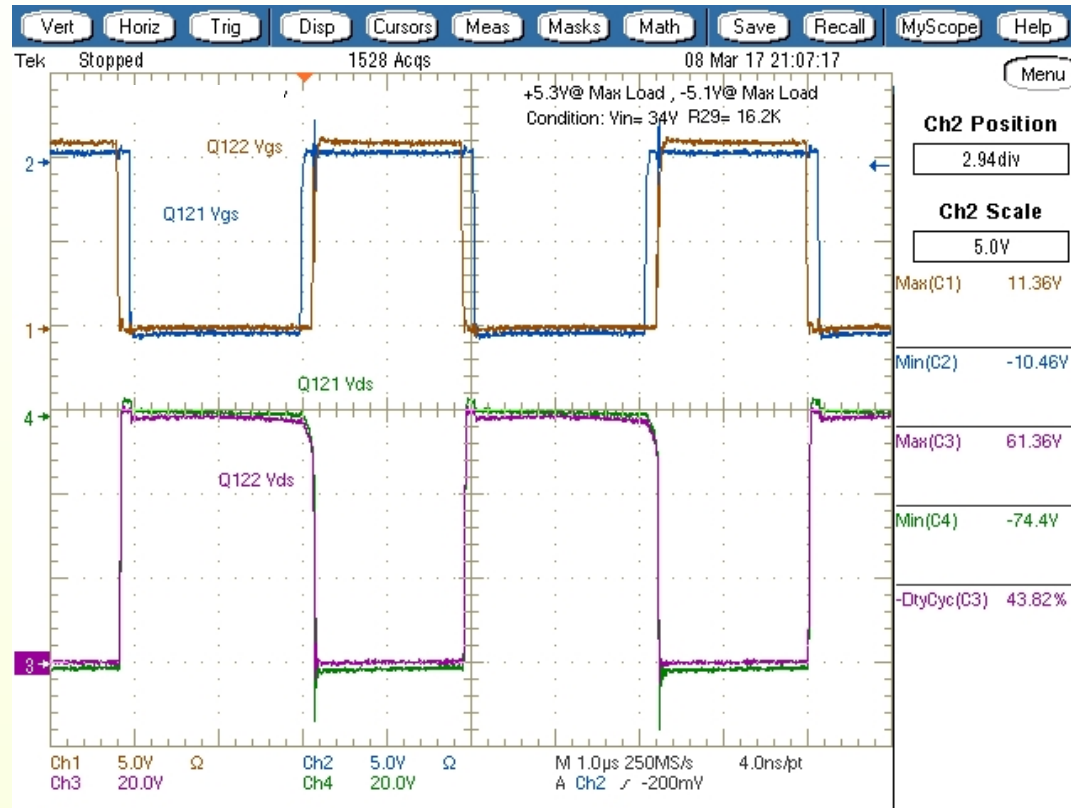


Loop



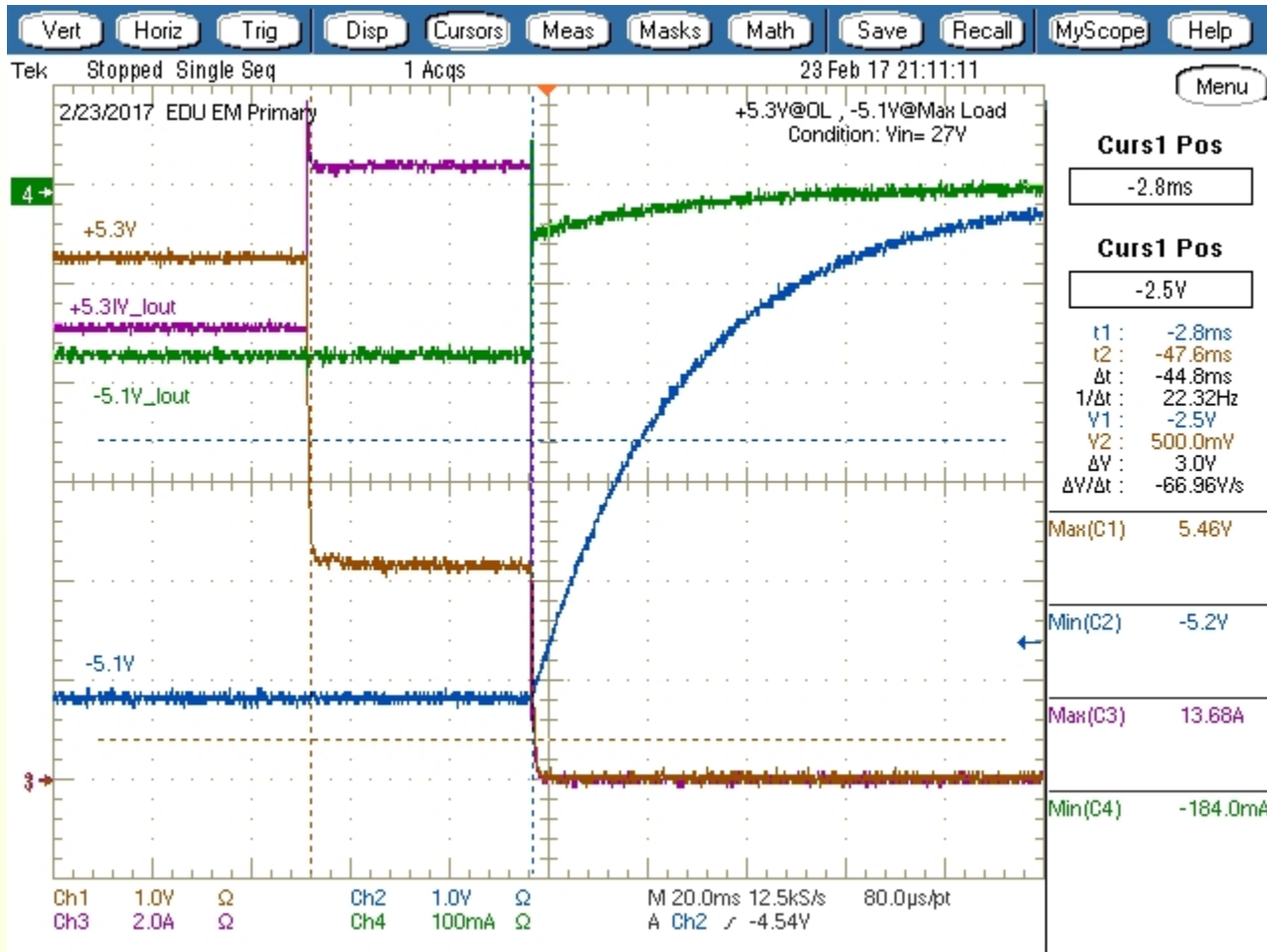
Hardware Test Results: BCMP

- Gate drive signals



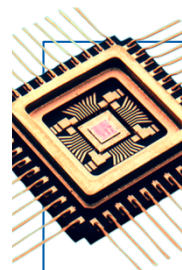
Clean waveforms indicate solid design

Peak Current Limit ASIC Waveforms: BCMP



Peak current limiter is fully functional

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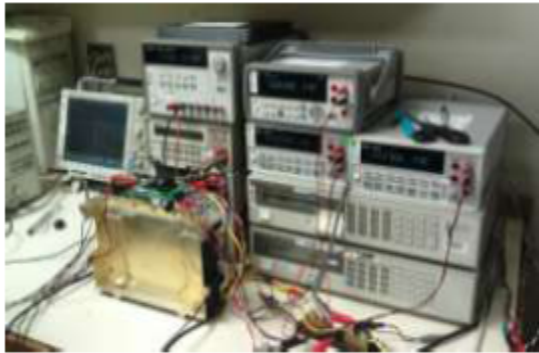


3. PwrCMOS ASICs: Radiation Test

- Completed TID/SEE tests
 - TID testing conducted at NGAS Radiation Test Operations Gamma Cell facility in Redondo Beach, CA
 - SEE testing conducted at the Texas A&M University (TAMU) Cyclotron Facility
- Test results meet all program requirements
 - TID test level > 30 kRad
 - SEL test level > 77.3 MeV
 - SEU: <1.0 x E-5 events per 30 days
- Further flight hardening is being pursued for
 - TID > 100 kRad

Radiation Test Setup

- NGAS Radiation Test Operations Gamma Cell facility



ASIC Test Set

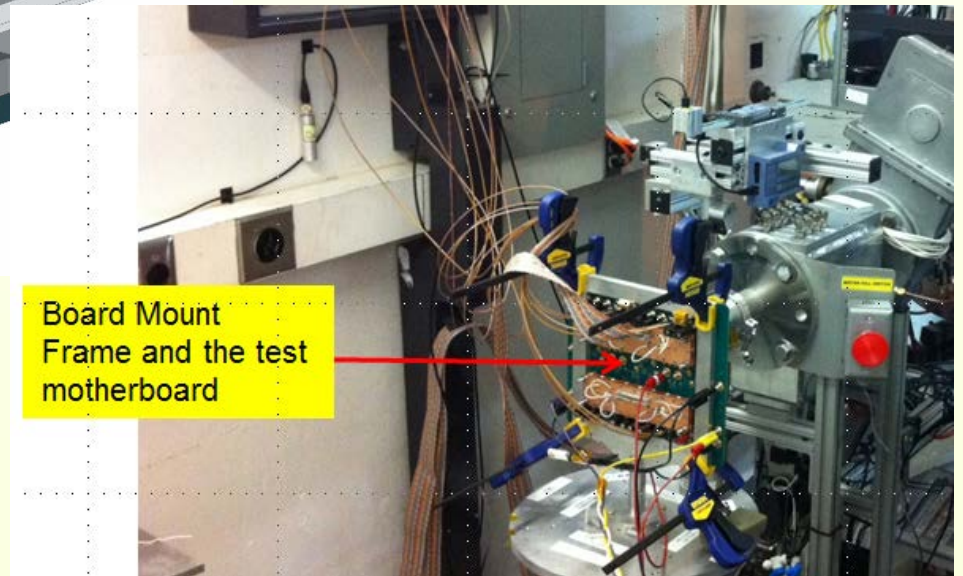
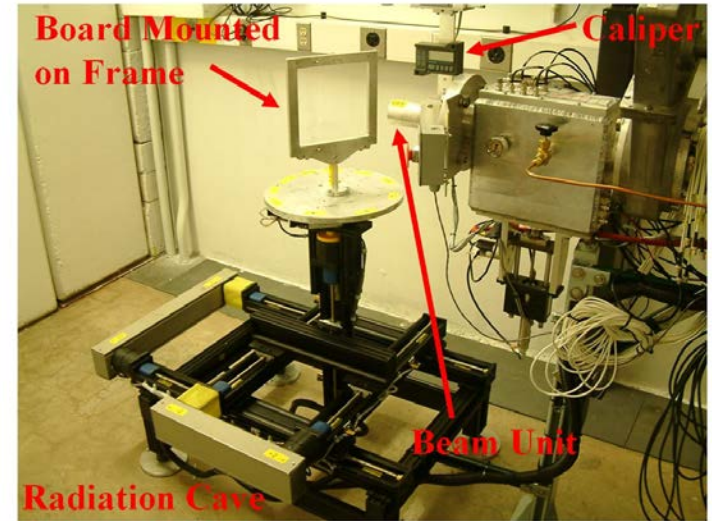
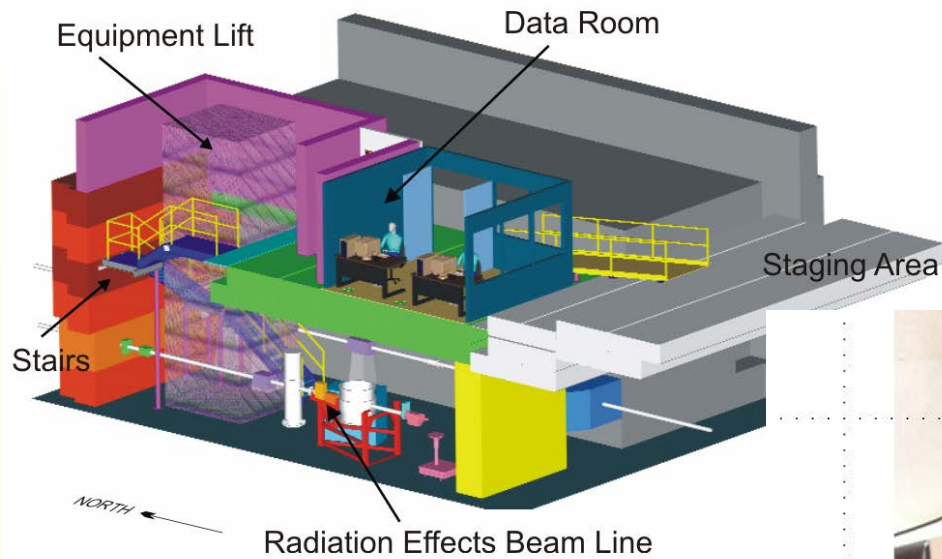
Power supplies, loads, meters, scope, fixture. Performs measurements pre-rad, post-rad, and provides bias to DUT during irradiation



Gamma Ray Source

Radiation Test Setup

- Texas A&M University (TAMU)
K500 Super Conducting Cyclotron Facility



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