Adiabatic Power Conversion (APOL) Technology Flight Insertion Status

THE VALUE OF PERFORMANCE.

NORTHROP GRUMMAN

March 20, 2019

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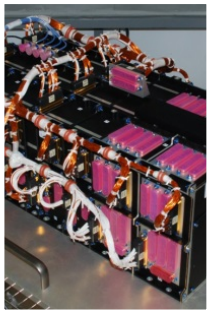
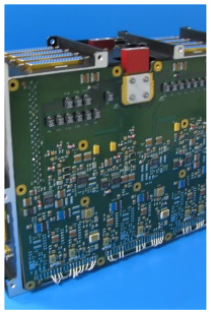
Outline



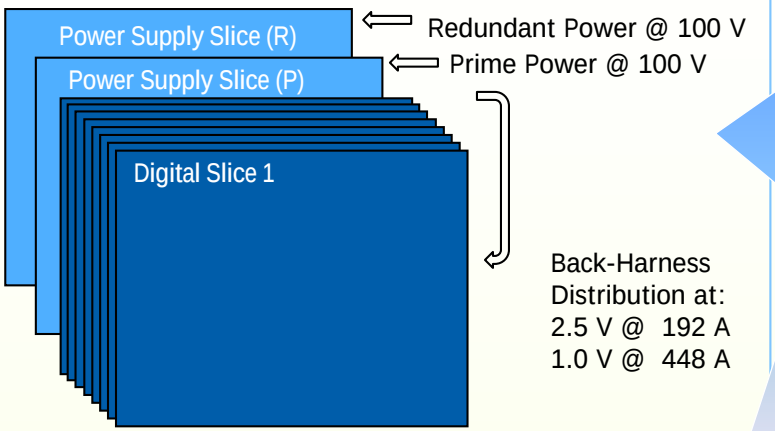
1. Double Regulated Intermediate Bus Architecture

2. Bus Converter Modules



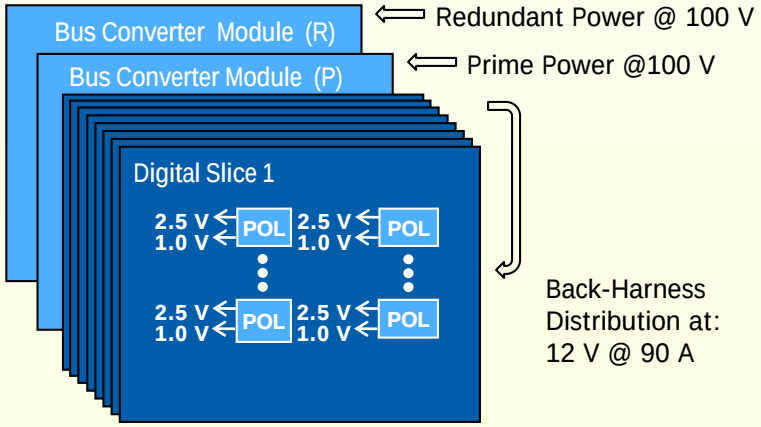
3. Point-of-Load Converters

APOL Technology



Centralized bus with one-step conversion

- **Problem**: With the increase of prime bus and the decrease of load voltage levels, the centralized architecture can no longer deliver the efficiency required
  - Excessive cable IR drops & weight
  - Significantly degraded power efficiency
- **Solution**: An intermediate power bus and ultra-efficient power converters
  - Reduction of 67% dissipation
  - Increase of 68% through power
  - Reduction of power generation, storage and thermal removal



Intermediate bus with two-step conversion

Performance	Centralized	DRIBA
Converter efficiency	75-85%	89-99%
End-to-end power distribution efficiency	65%	>85%
Size reduction	-	>2x
Producibility	Poor	Good
Testability	Poor	Good

Adiabatic Power Conversion Accomplishment

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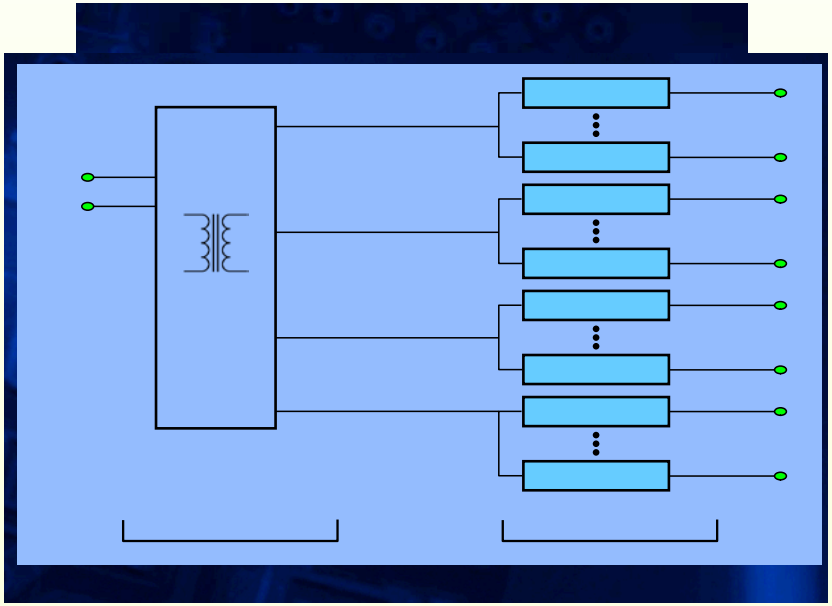
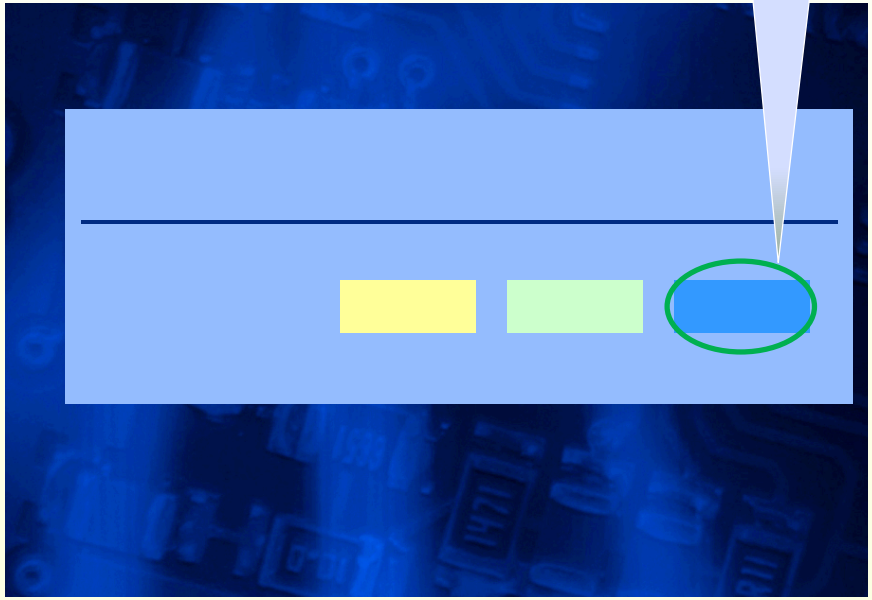
Adiabatic Technology Construct:

1. Double regulated intermediate bus
2. Extremely efficient power converter
3. Low-power, high functionality PwrCMOS ASICs

	Measured Best Efficiency at 1/3 Load (%)	Measured Min Efficiency at Full Load (%)
APOL EM	97.1	95.2
APOL BCM EM	92.6	92.1
End-to-End	89.9	87.7

As previously presented, we accomplished all we set out to do on the APOL Program within schedule/cost





Double Regulated Intermediate Bus Architecture (DRIBA) Provides a Discriminating Technology Construct for Adiabatic Power Conversion, particularly for High Power/Low Voltage

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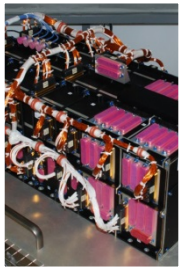
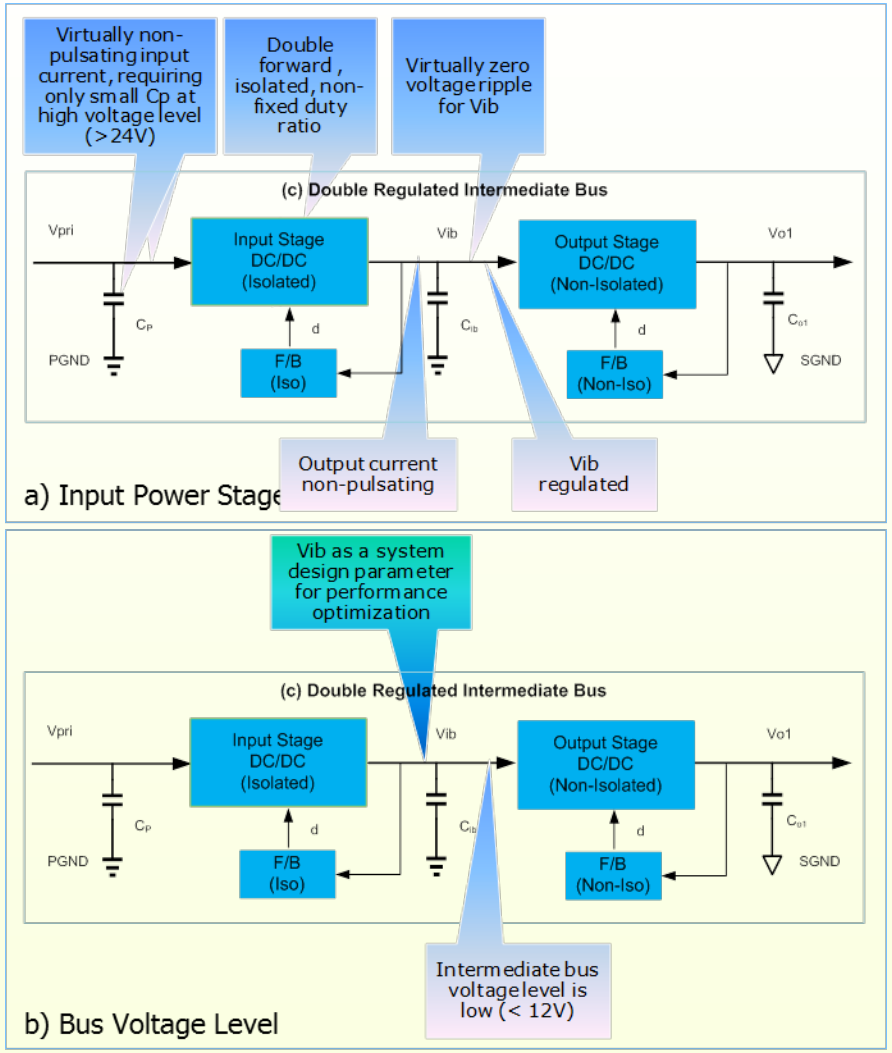


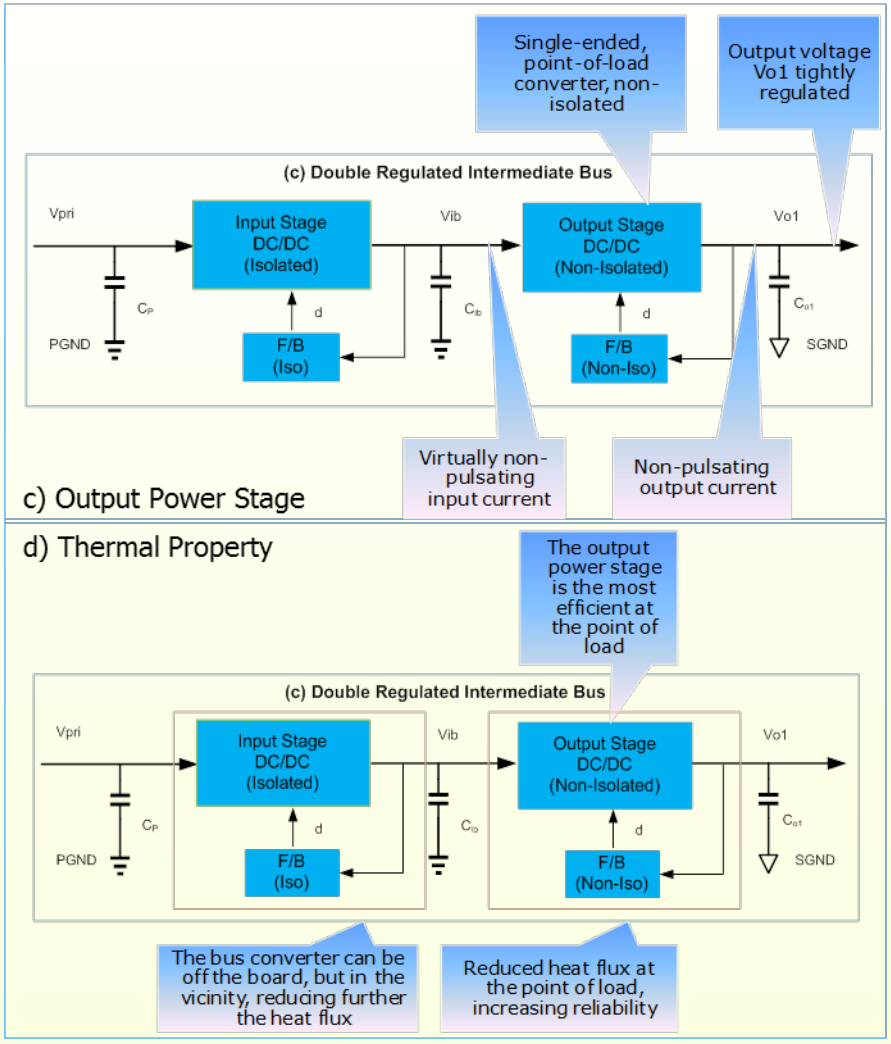
1. Double Regulated Intermediate Bus Architecture

DRIBA Key Advantages



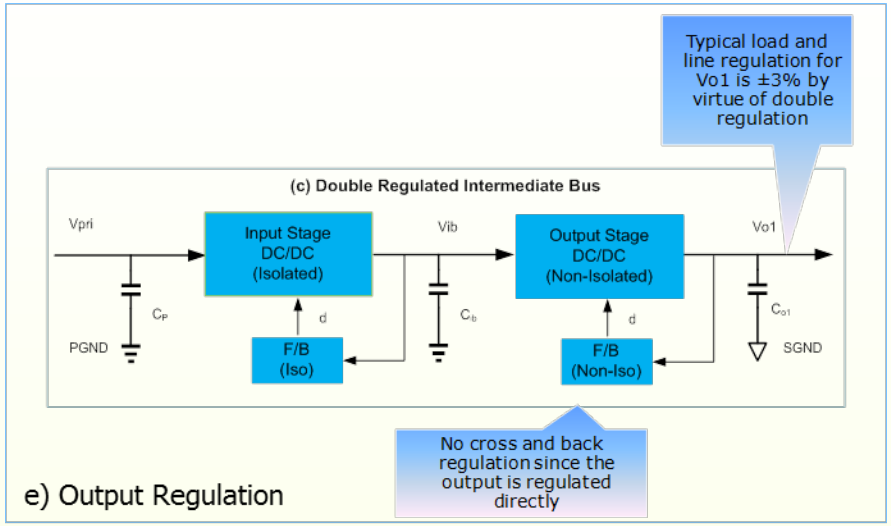
A significant departure from prior approaches is the ability to use the intermediate bus voltage to optimize at the system level

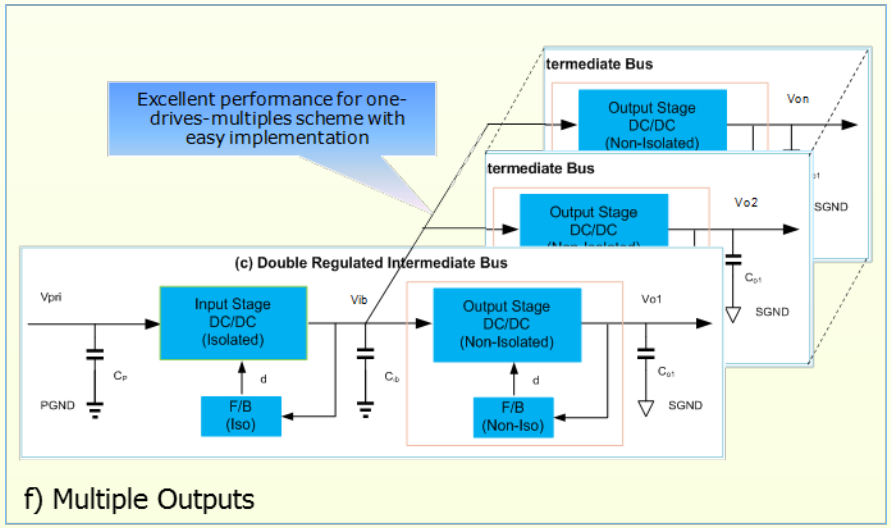
DRIBA Key Advantages (cont'd)



Virtually non-pulsating current at the intermediate bus and at the output

DRIBA Key Advantages (cont'd)





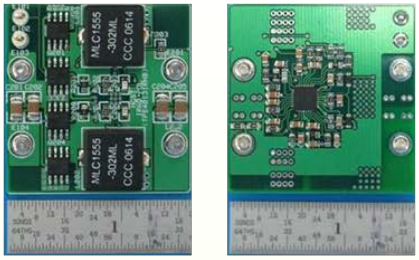
Easy paralleling for multiple outputs with tight regulation

Comparison of Various Architectures

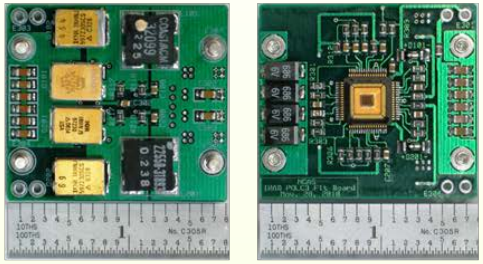
	Input Power Stage	Intermediate Bus Voltage Level	Output Power Stage	Thermal Property	Regulation	Multiple Outputs	System Stability & Output Impedance
Regulated	• Single ended, Buck or Buck-Boost, • Pulsating input current with large cap at bus voltage level (usually >24 V) • Output current can be pulsating • Regulated	High, usually > 12V	• Double ended, push-pull, half or full bridge • Virtually non-pulsating input current • Virtually non-pulsating output current • Unregulated	• Most efficient power stage not at output • Increase of point-of-load heat flux • Reduced reliability	• Typical load/line regulation <±10% • Cross regulation is large • Back regulation is large	• Poor, >±10%, typical	• Favorable in stability • Output impedance high
Unregulated	• Double ended, half or full bridge as bus converter • Virtually non-pulsating input current • Non-pulsating output current • Unregulated with fixed duty ratio	Low, usually < 12V	• Single ended point of load (POL) • Pulsating input current • Non-pulsating output current • Regulated	• Most efficient power stage at the output • Reduced point-of-load heat flux • Increased reliability	• Typical load/line regulation <±7% • No cross regulation • No back regulation	• Good, ±5 -7 %, typical	• Not favorable in stability • Output impedance low
Double Regulated	• Hybrid • Virtually non-pulsating input current • Non-pulsating output current • Virtually zero voltage ripple • Output regulated	• Low, usually < 12V • Value as a design parameter for max system performance	• Hybrid • Virtually non-pulsating input current • Non-pulsating output current • Output regulated	• Most efficient power stage at the output • Reduced point-of-load heat flux • Increased reliability	• Typical load/line regulation <±3% • No cross regulation • No back regulation	• Excellent, <±5%, typical	• Favorable in stability • Output impedance low

*** - D. Tan, "A review of intermediate bus architecture: a system perspective,"** ***IEEE Journal of Emerging and Selected Topics inn Power Electronics,*** **Vol. 2, No. 3, Sep., 2014, PP. 363-373**

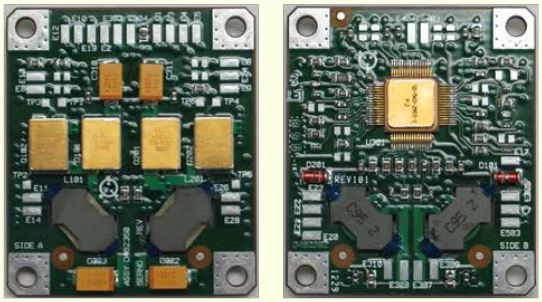
APOL Generic EM Hardware



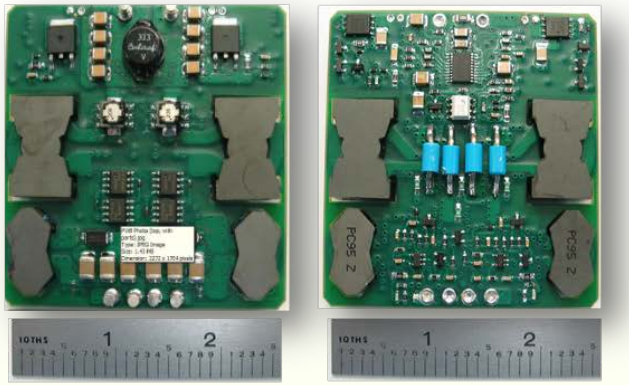
a) APOL Breadboard



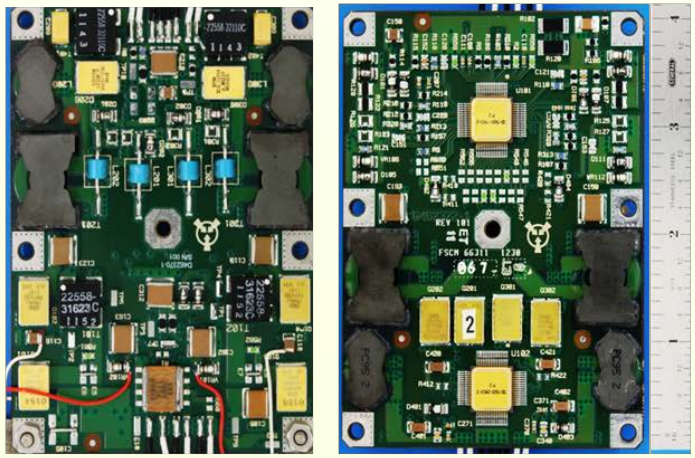
a) APOL Brassboard



c) APOL Engineering Model



a) BCM Brassboard



b) BCM Engineering Model

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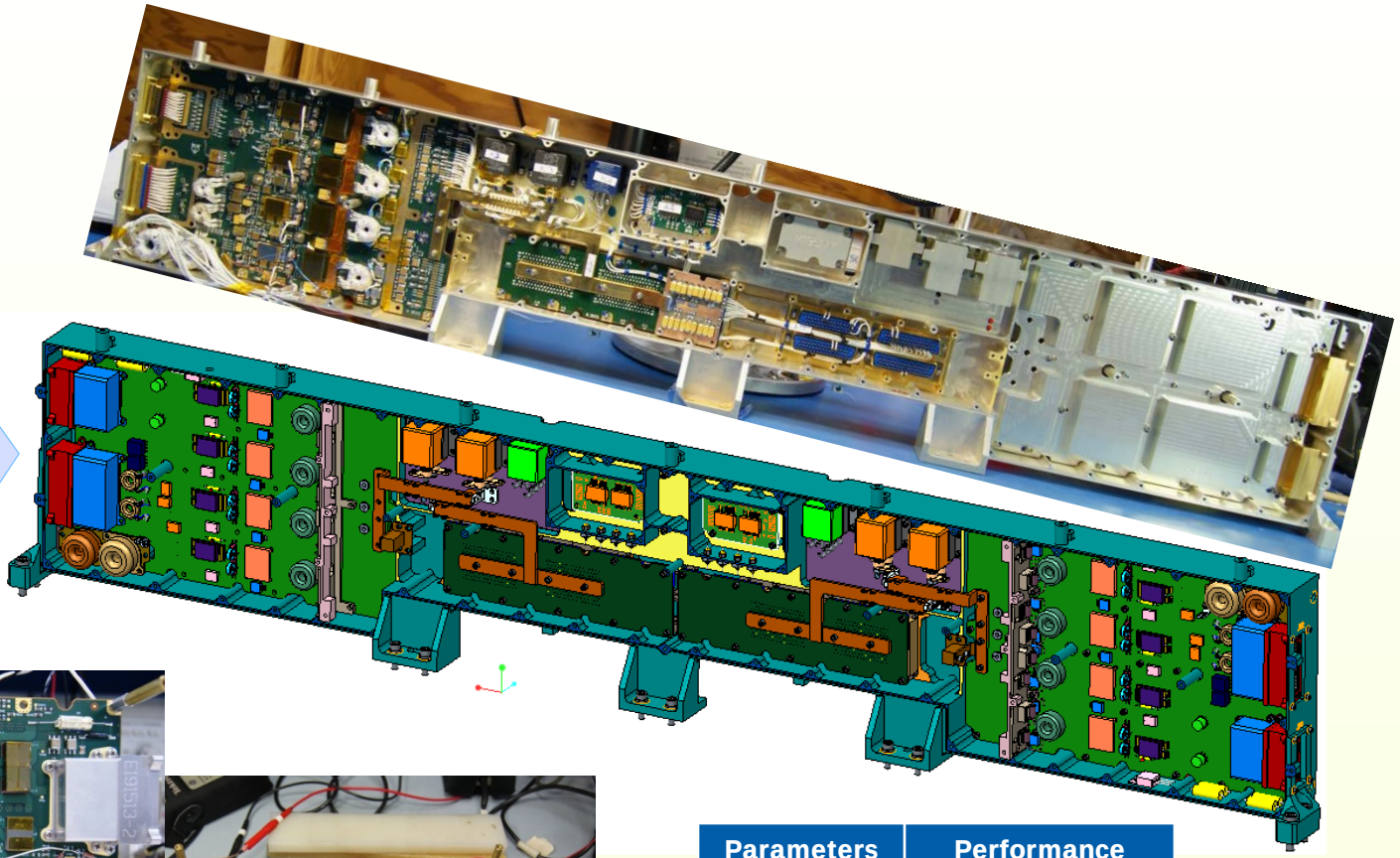
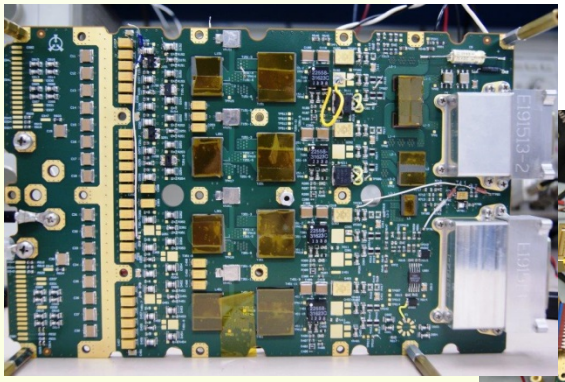
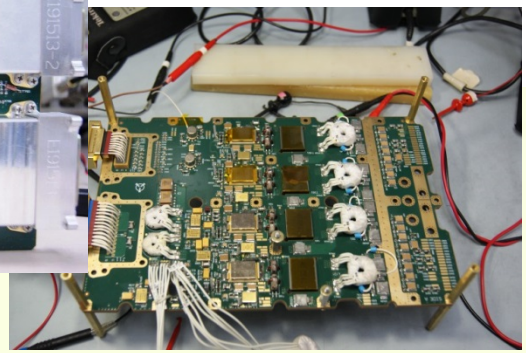
2. Flight Insertion: BUS (Isolated) Converter Modules

Isolated Converters: ECA

Key Features:
- Single-board assembly for superior manufacturability and testability
- Fully embedded planar magnetics
- Dedicated PwrCMOS ASICs
- High EMI performance
- High efficiency
- Fully redundant design







Parameters	Performance
Vin (V)	27 - 34
Vo	6.3V at 4x16=84A
Size (in3)	7.8x8.0x11.0
Efficiency (%)	86

Isolated Converters: ECA Performance

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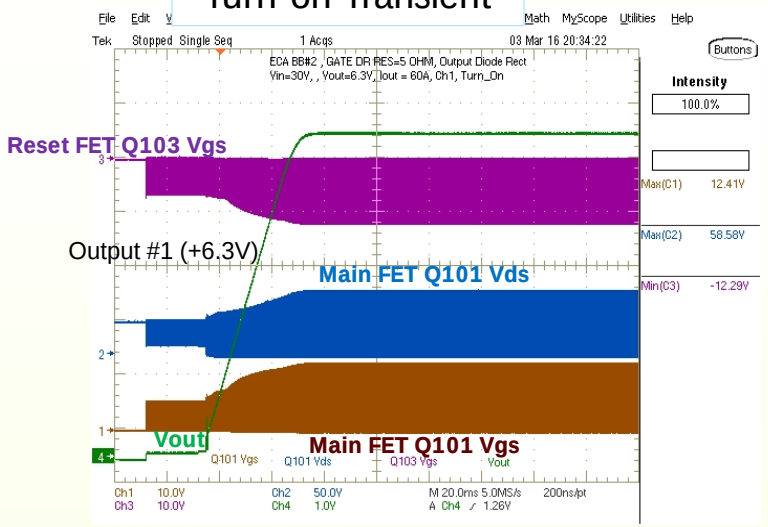
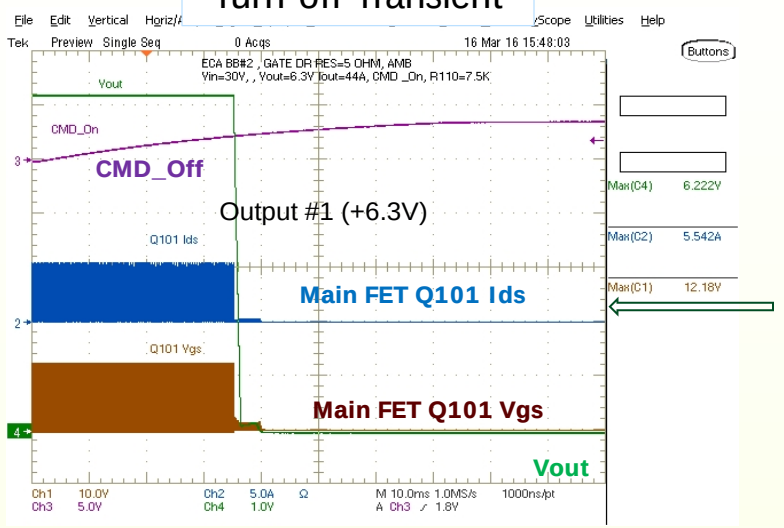
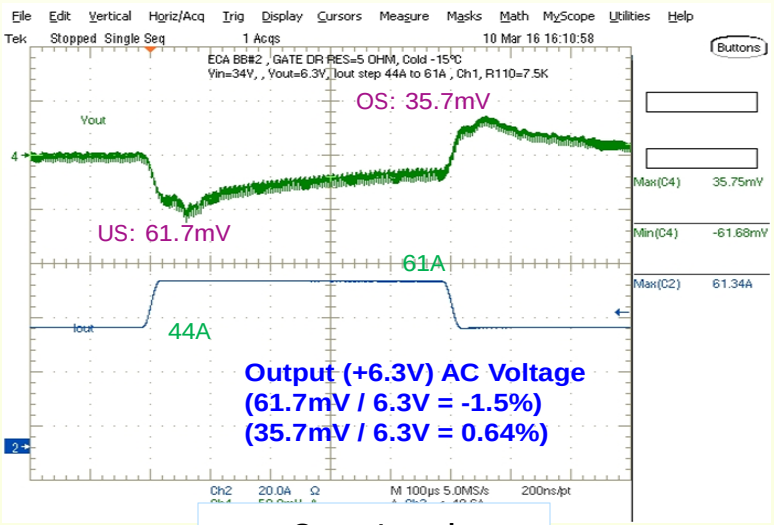
Turn-on Transient

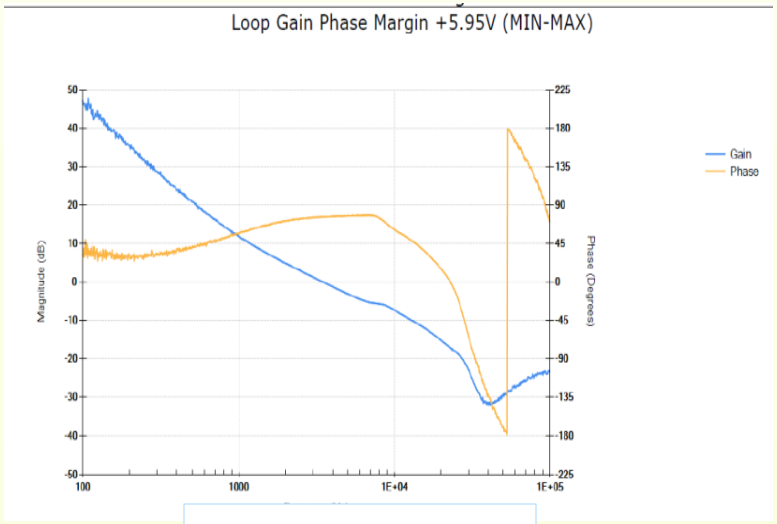


Turn-off Transient





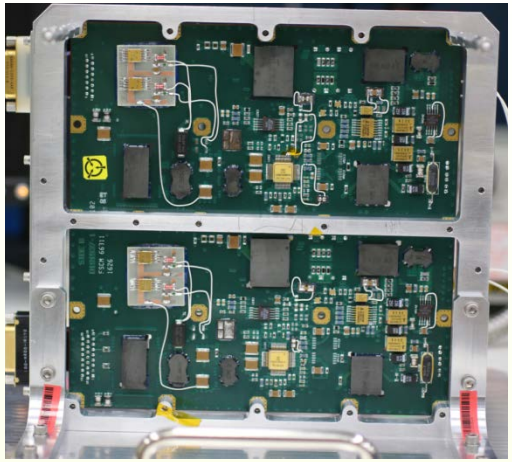
Step Load

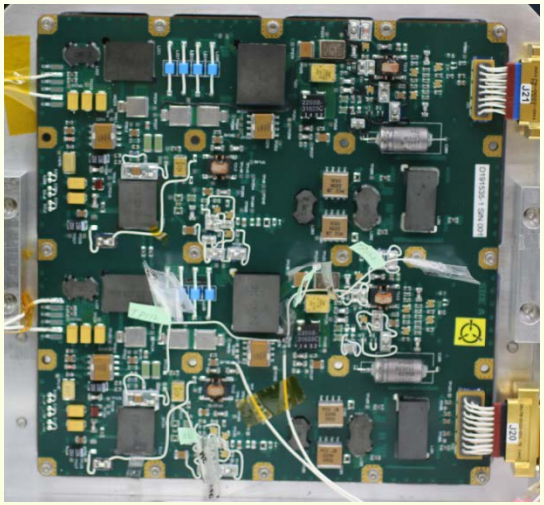


Loop

Isolated Converters: EDU

Key Features:
- Single-board assembly for superior manufacturability and testability
- Fully embedded planar magnetics
- Dedicated PwrCMOS ASICs
- High EMI performance
- High efficiency
- Fully redundant design





EDU FM

Parameters	Performance
Vin (V)	27 - 34
Vo	5.3V at 4.6A
	-5.1V at 0.19A
Size (in3)	
Efficiency (%)	83

Isolated Converters: EDU Performance

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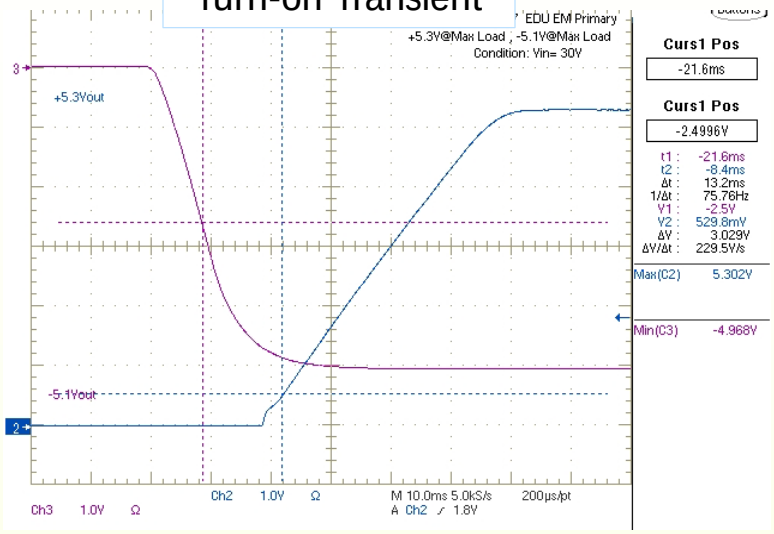
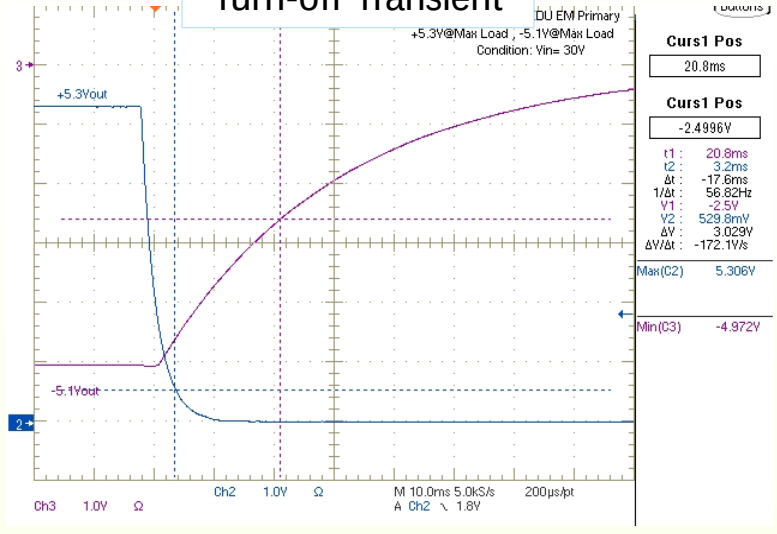
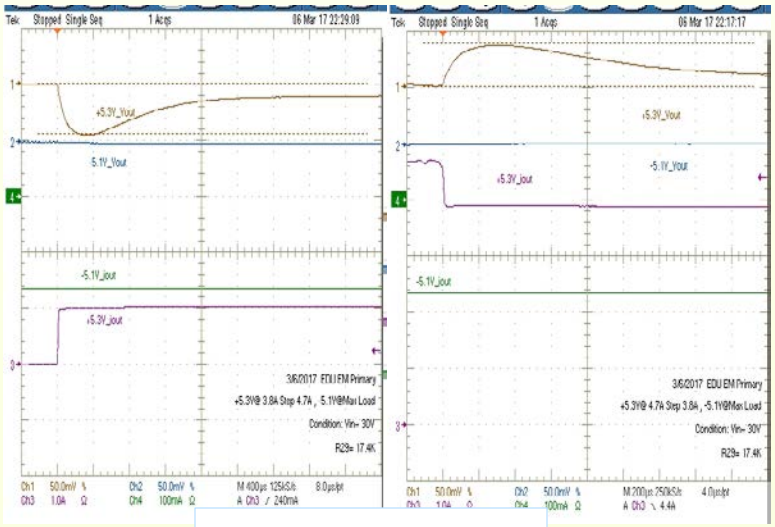
Turn-on Transient



Turn-off Transient





Step Load

Loop

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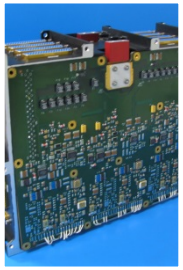
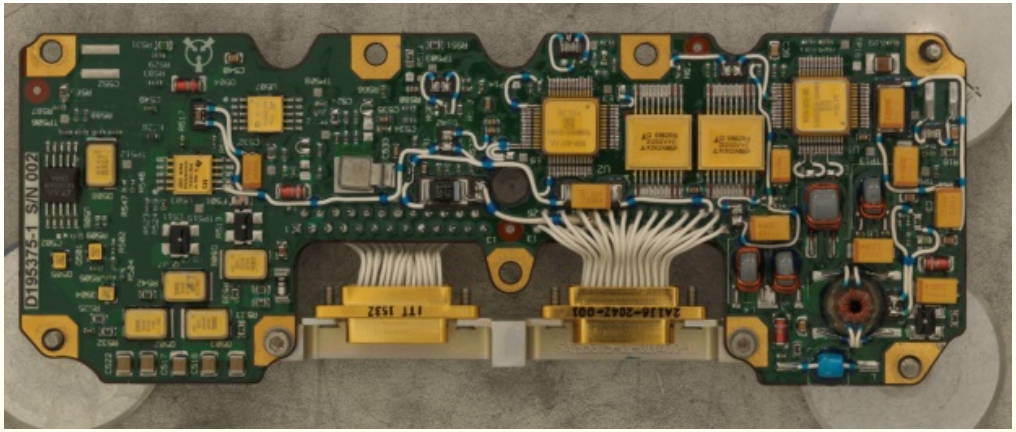


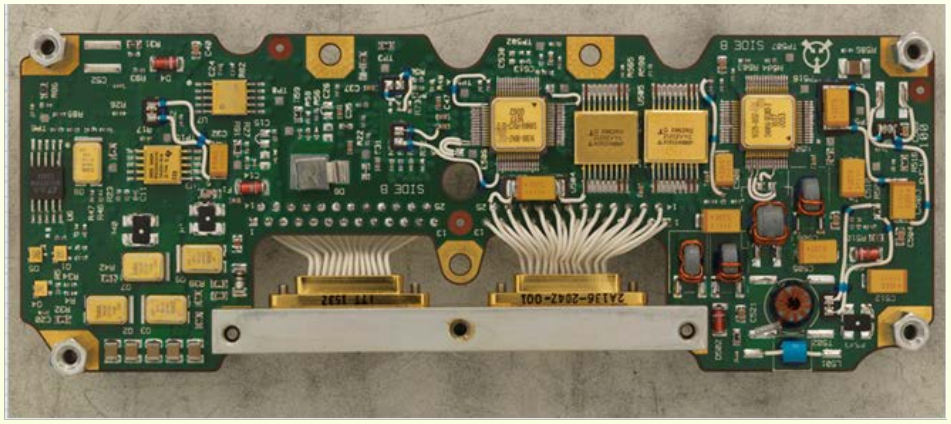
3. Flight Insertion: Point-of-Load Converters

Point-of-Load Converters: POL-A

Parameters	Performance
Input	4.9 – 5.2 V
Output(s)	3.3V at 1.15A
	1.82V at 0.82A
	-5.0V at 0.022A
Size (in3)	7.2x1.9x8.0
Efficiency (%)	83

POL-A Flight





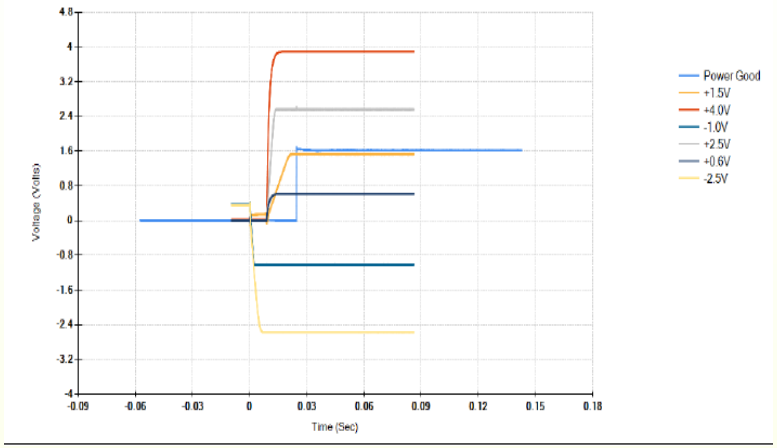
POL-A EM

Key Features:

- Single-board assembly for superior manufacturability and testability
- Fully embedded planar magnetics
- Dedicated PwrCMOS ASICs
- High EMI performance
- High efficiency
- Fully redundant design

Point-of-Load Converters: POL-A Performance

Turn-on Transient



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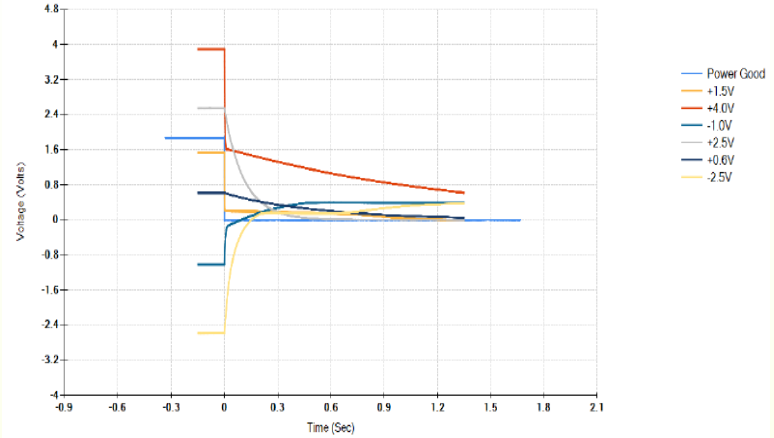
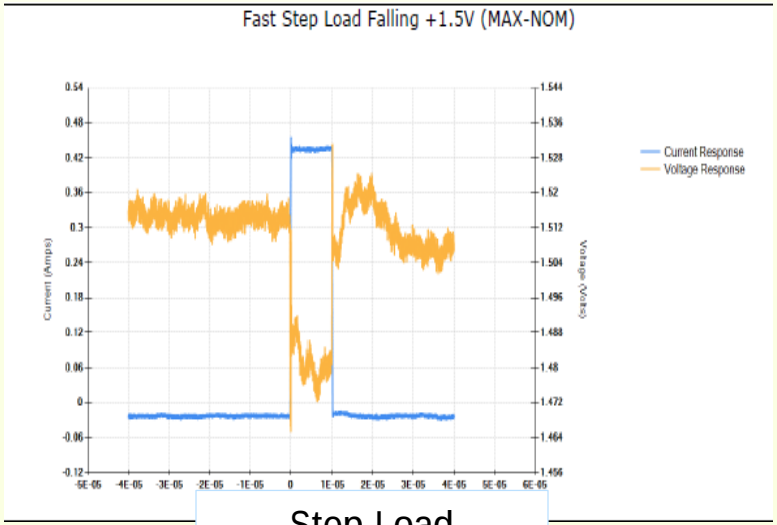
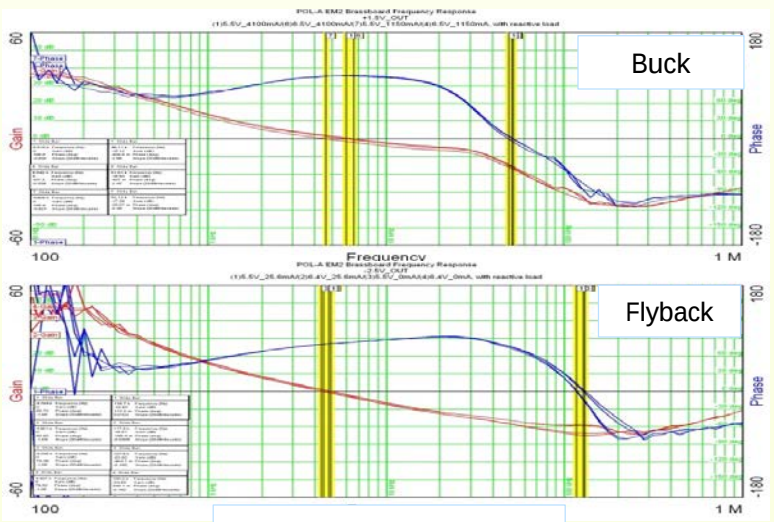


Step Load

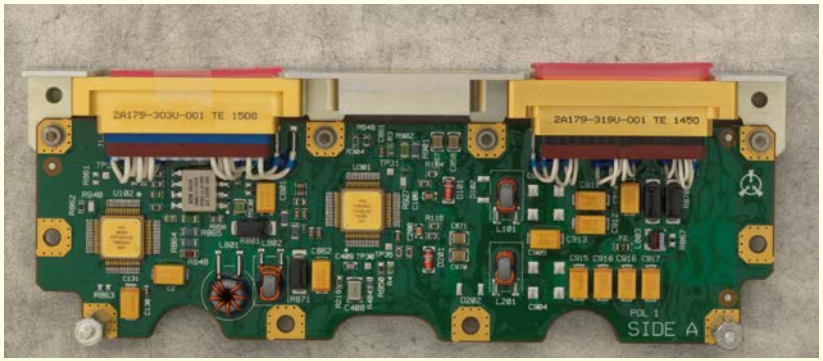


Loop



Point-of-Load Converters: POL-1

Key Features:
- Single-board assembly for superior manufacturability and testability
- Fully embedded planar magnetics
- Dedicated PwrCMOS ASICs
- High EMI performance
- High efficiency
- Fully redundant design



POL-1 Flight

Parameters	Performance
Input	4.9 – 5.2 V
Output(s)	3.3V at 1.15A
	1.82V at 0.82A
	-5.0V at 0.022A
Size (in3)	2.47 x 0.5 x 6.68
Efficiency (%)	83

Point-of-Load Converters: POL-1 Performance

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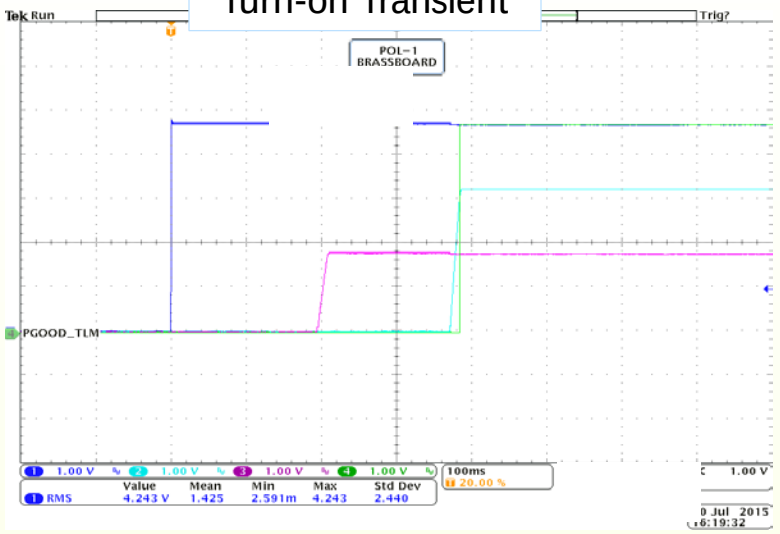
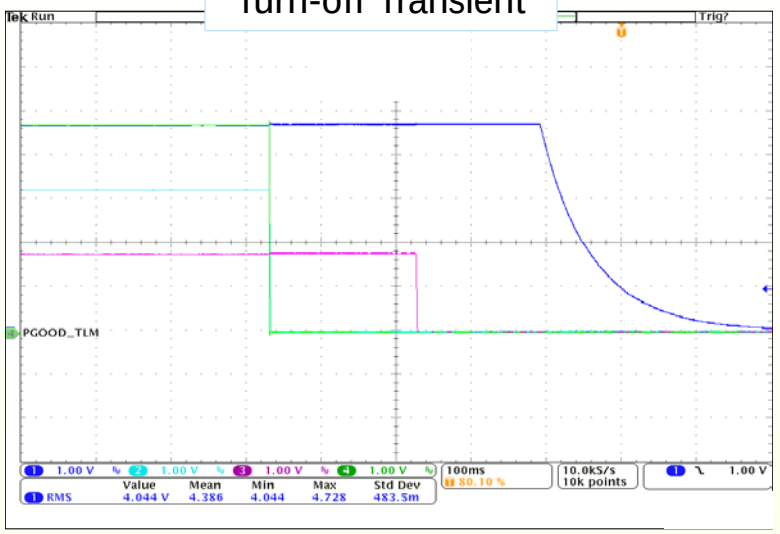
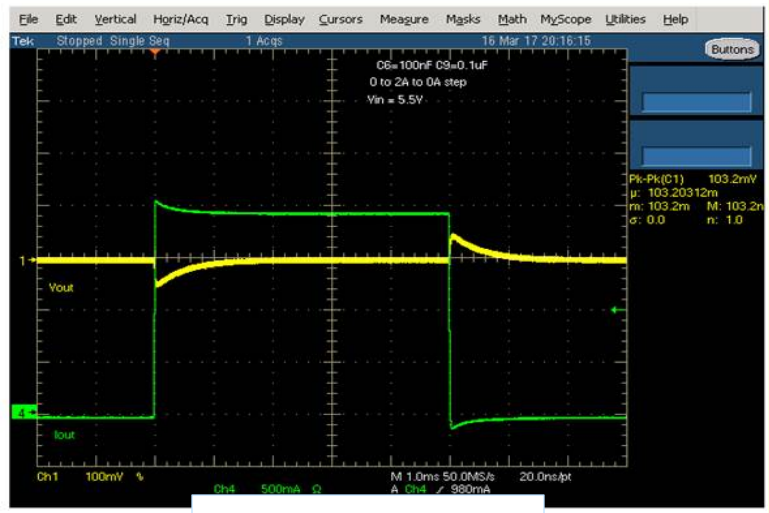
Turn-on Transient

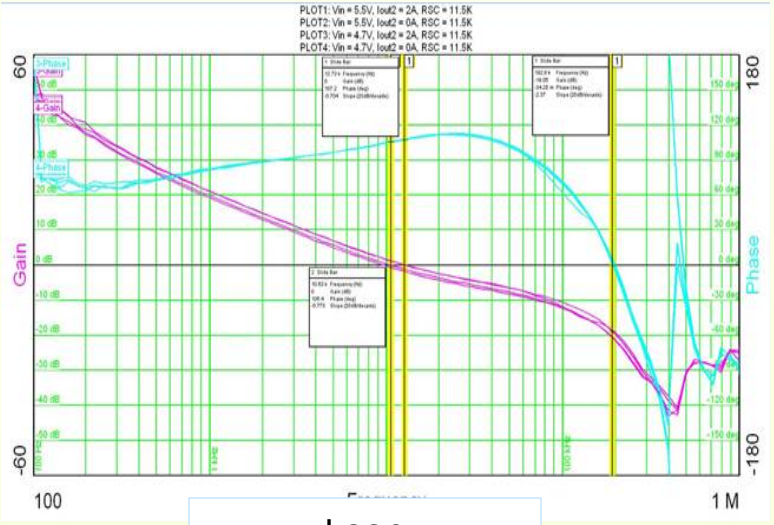


Turn-off Transient





Step Load

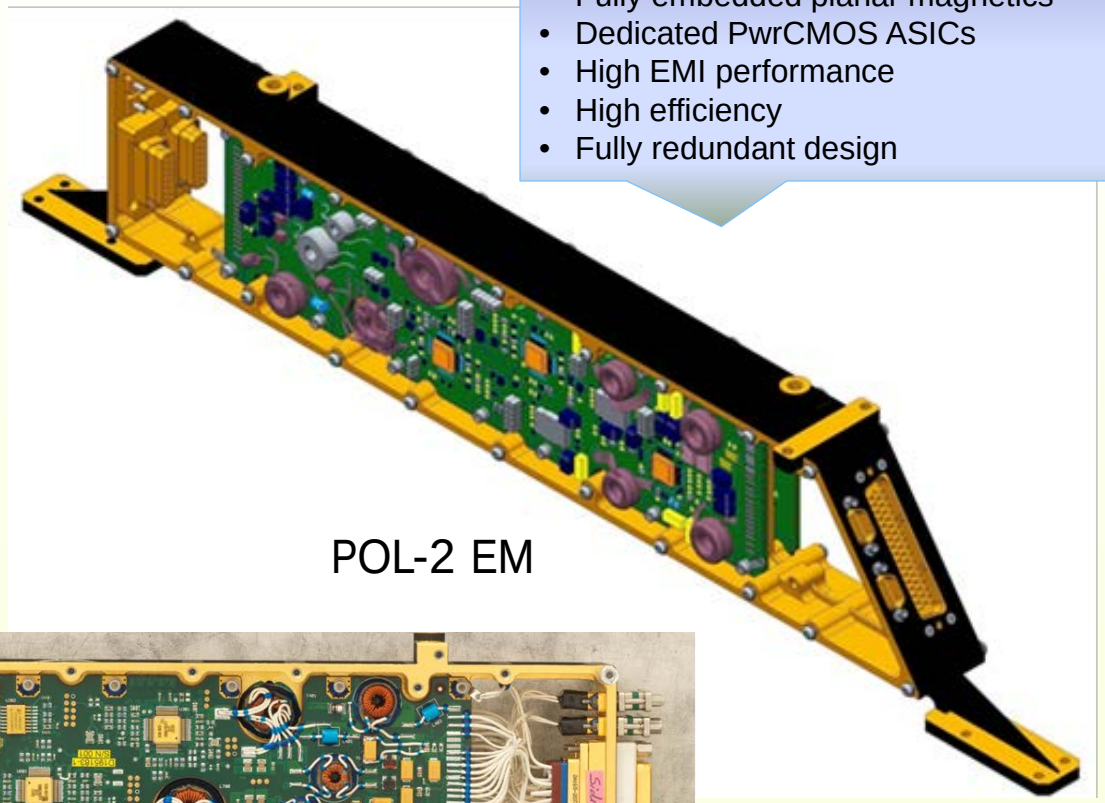


Loop

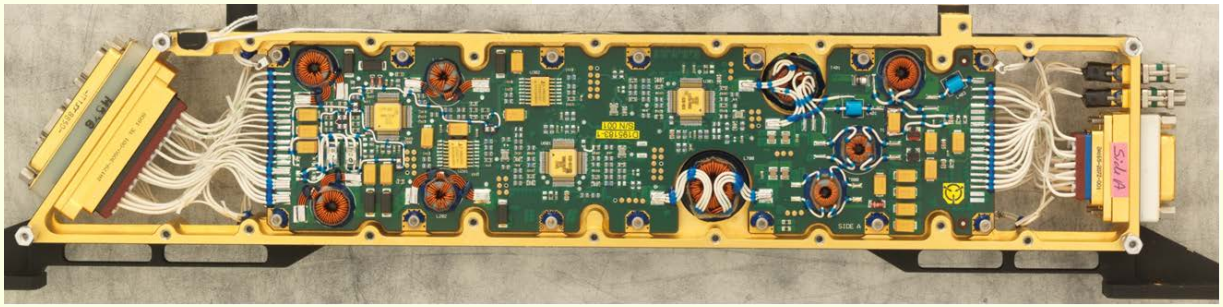
Point-of-Load Converters: POL-2

Parameters	Performance
Input	5.5 – 6.2 V
Output(s)	4.2V at 0.016A
	-1.0V at 0.246A
	5.15V at 0.786A
	6.5V at 0.025A
	4.0V at 4.16A
Size (in3)	20.45 x 4.265 x 1.8
Efficiency (%)	86

Key Features:
- Single-board assembly for superior manufacturability and testability
- Fully embedded planar magnetics
- Dedicated PwrCMOS ASICs
- High EMI performance
- High efficiency
- Fully redundant design



POL-2 EM



Point-of-Load Converters: POL-2 Performance

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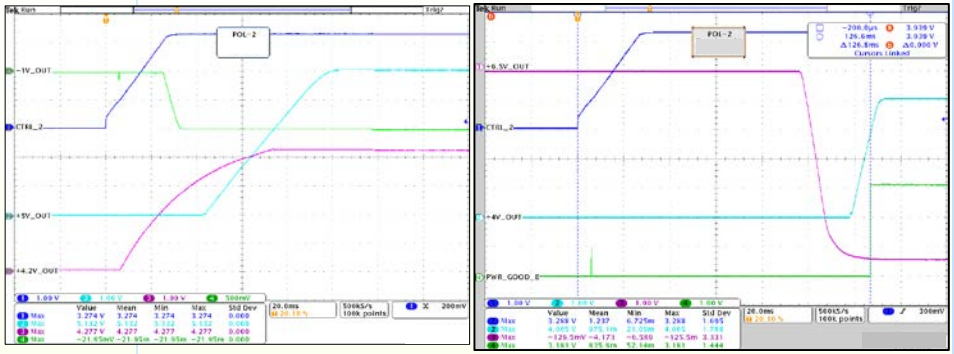
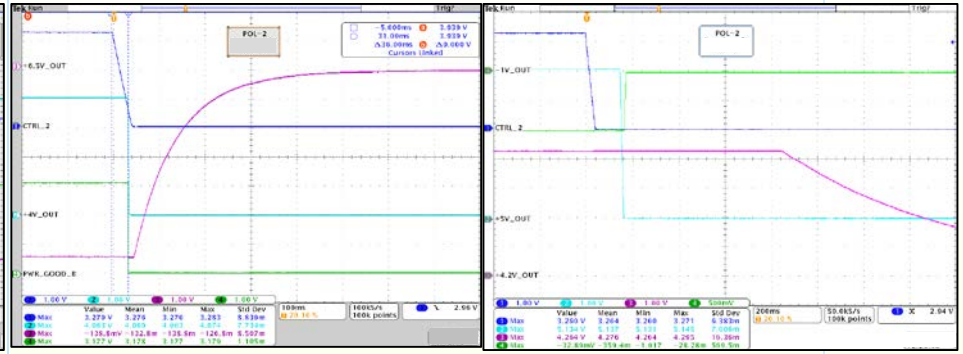
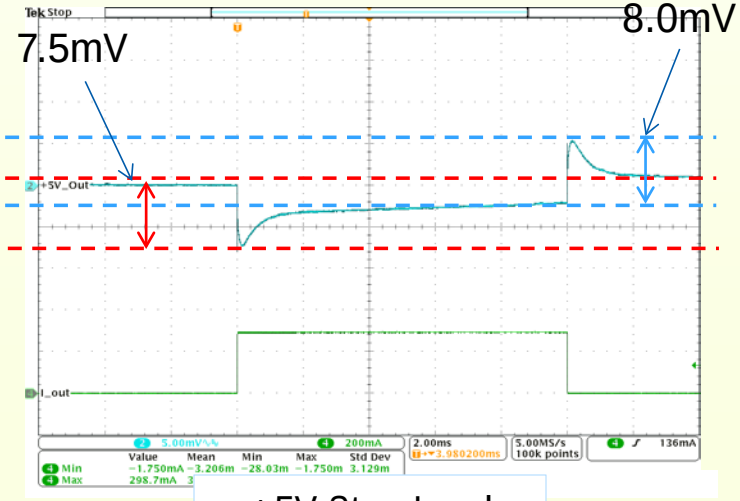
Turn-on Transient

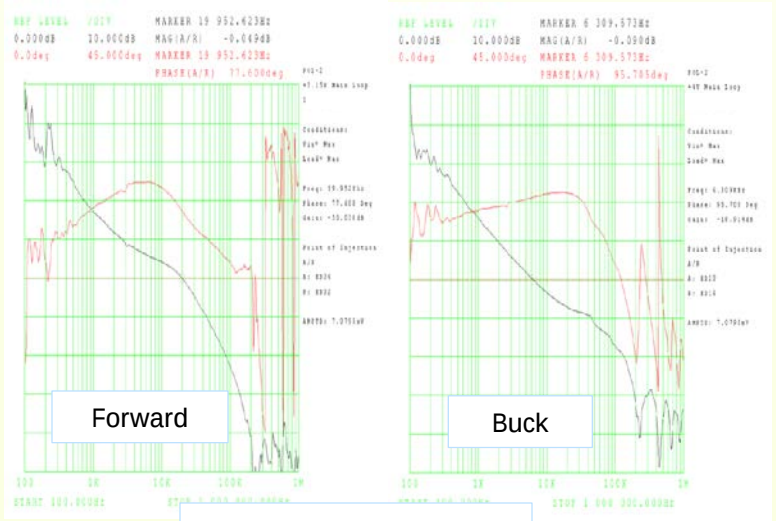


Turn-off Transient





+5V Step Load



Loop


THE VALUE OF PERFORMANCE.
NORTHROP GRUMMAN