# Lessons Learned from Power Integrity

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ae systems
ANALYTICAL HEAVY LIFTING

# PI is Not My Problem

**"Power is not my problem, its yours."**
*-- high speed designer*

**"What do you want, I gave you 5Vdc?!?!"**
*-- power supply designer*

**Dirty Secret: They're both wrong.**

**Power is everyone's problem.**

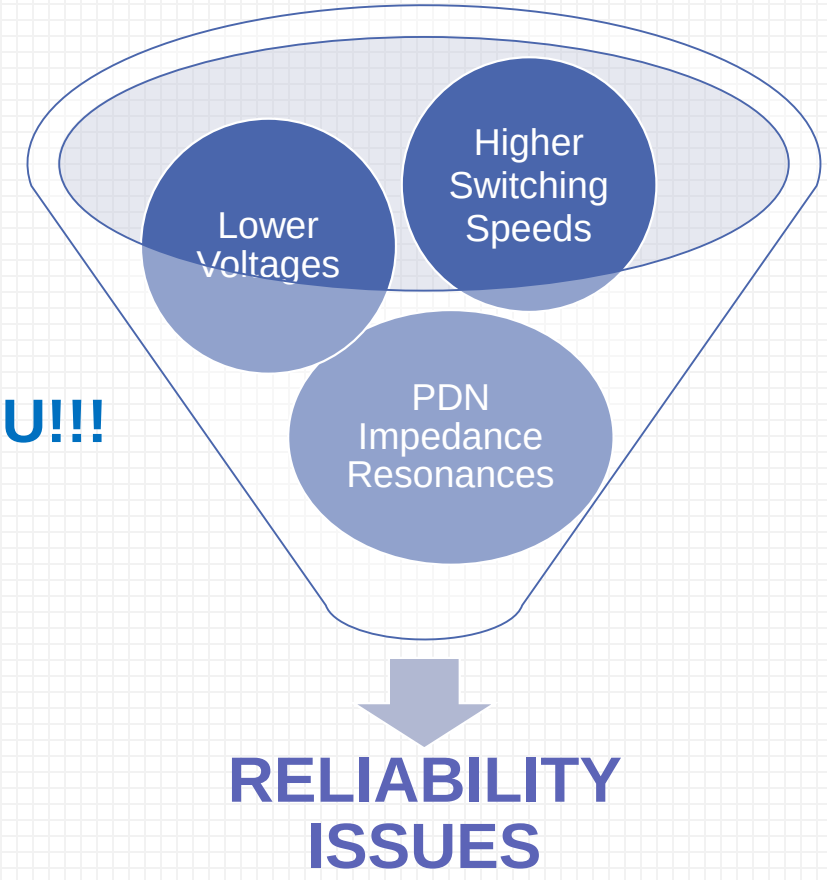
Power Supply Designers & Manufacturers | PCB Designers | Circuit Designers

# Power Integrity Applies to Everyone

- **Power Integrity is about getting the right power to the load**

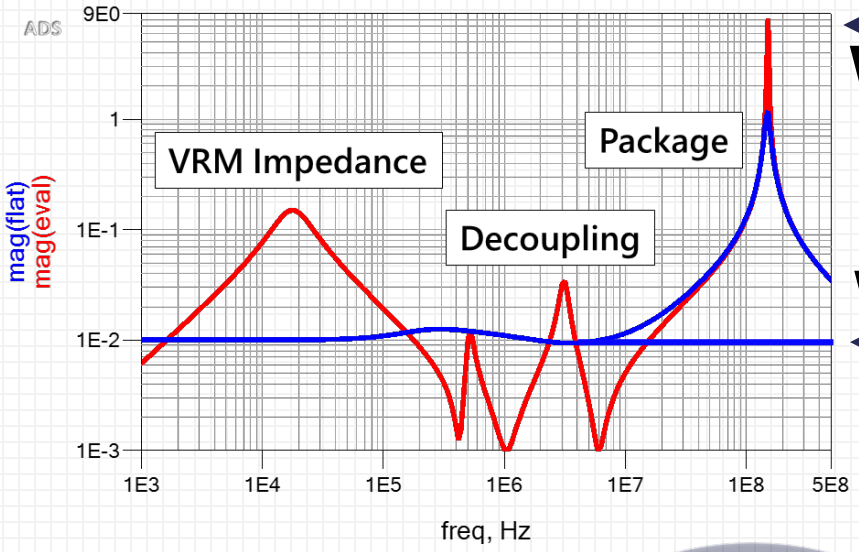
- **PI is NOT A SYSTEM ISSUE!**
- **PI is NOT A HIGH-SPEED ISSUE!**
- **PI is NOT A POWER SUPPLY ISSUE!**
- **It is an EVERYONE issue - YES, IT APPLIES TO YOU!!!**

- **Overstress and regulation issues? Sure.**
- **Dynamic current issues? Sure.**
- **Low current issues? Sure.**
- **Jitter issues? Sure.**
- **Heritage design issues? Sure.**




*"The Unfortunate State of Power Integrity in Space Systems" – Space Power Workshop 2017*

# The Power Distribution Network (PDN)

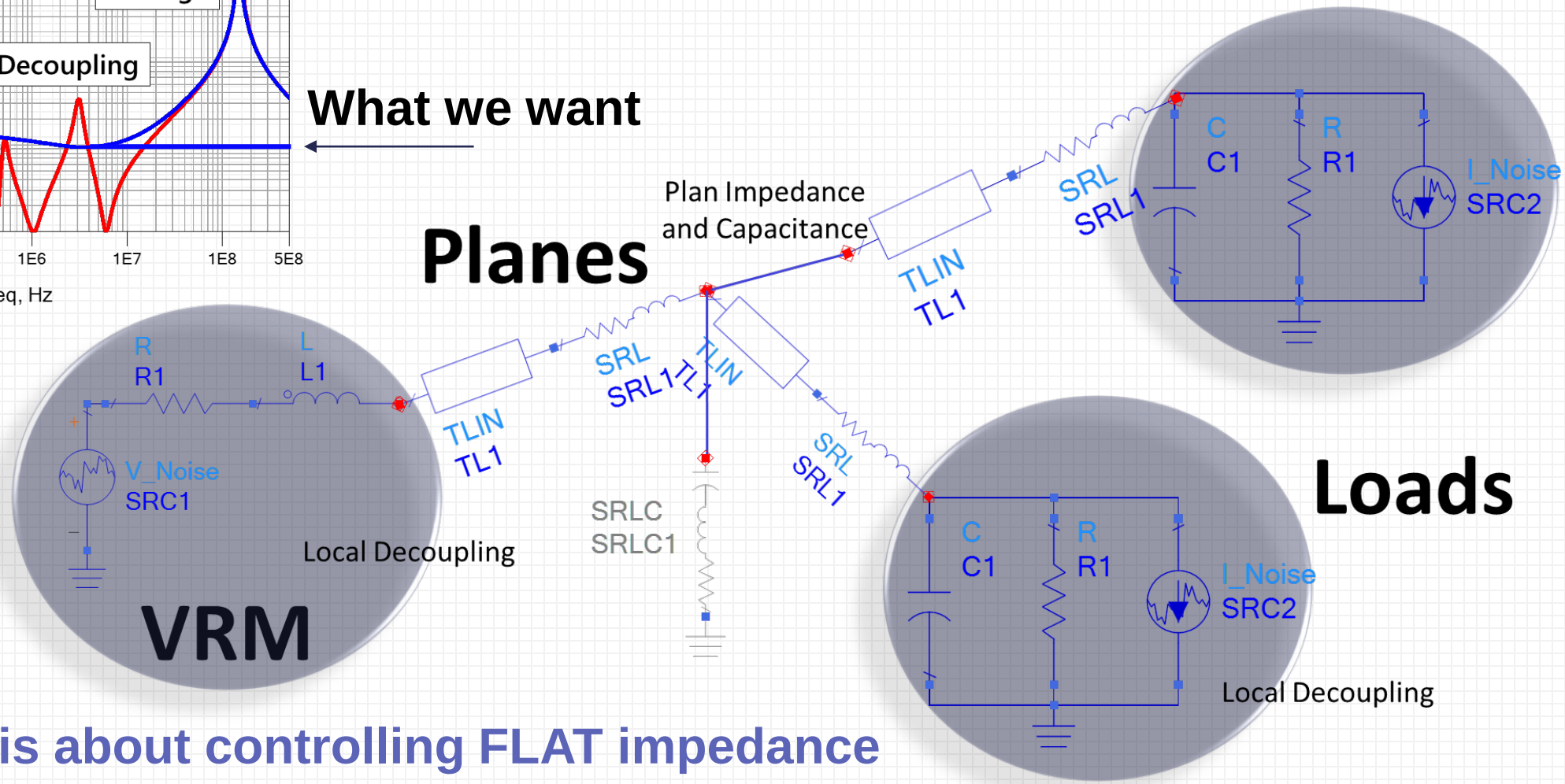



**What we get**

**What we want**

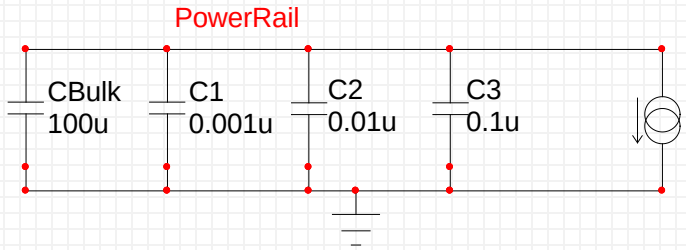
**Planes**

Plan Impedance and Capacitance

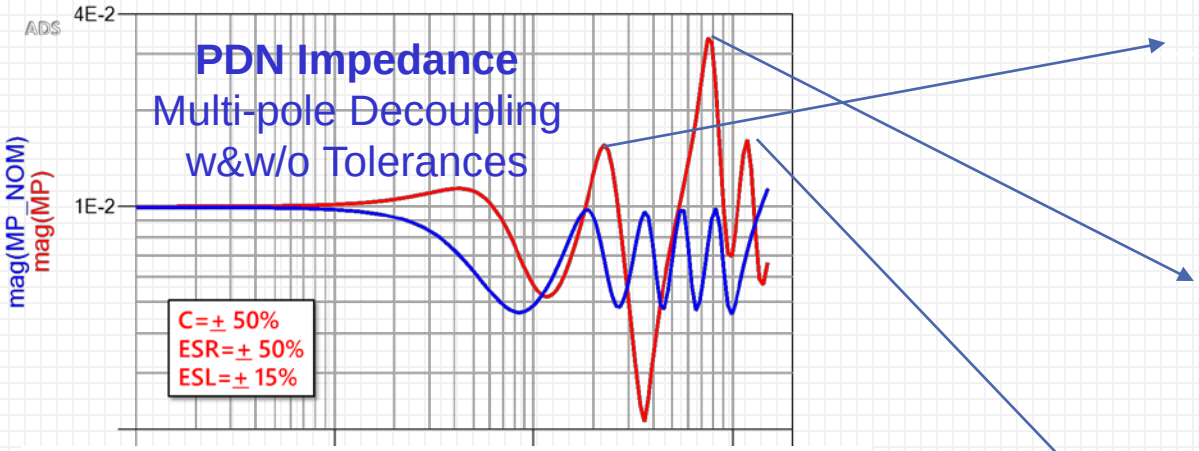


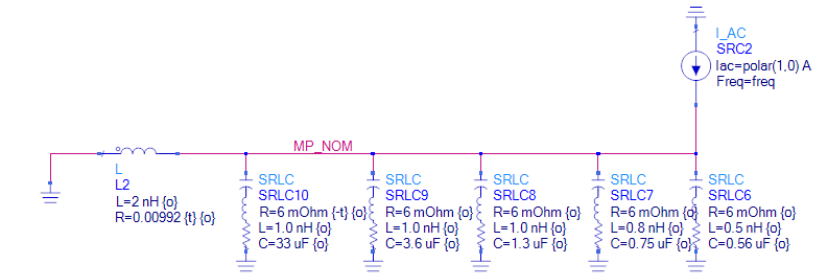

**Power Integrity is about controlling FLAT impedance**

# The Basic Problem: How we get into trouble



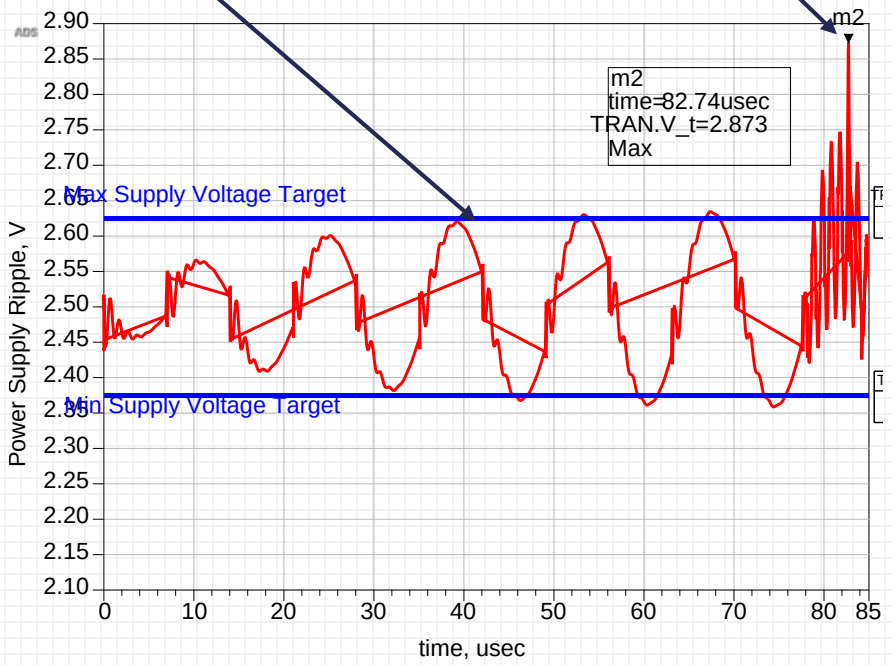

**But this what we build!**




**Poor Power Integrity Design**

**This is the spec**




**DC + Ripple + CS + SL + Noise < 5% of Vsup**

# Fighting a Lack of Data

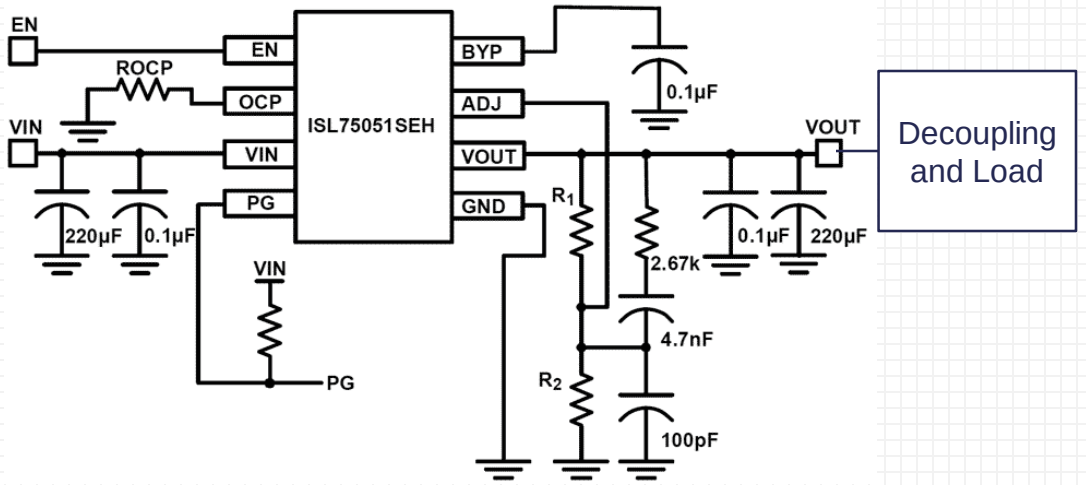
- **These things are impacting designs and they need to be considered and addressed**
- **Impedance is how we communicate – it's the answer**
  - IC manufacturers need to provide the output impedance data
  - VRM Models need to reflect accurate output impedance and they usually don't - RL models are a minimum
  - Capacitor models are often bandwidth limited and not measured using a 2-port measurement
- **Impedance needs to be Flat**
  - There's a VRM, a plane, and a load. How do we make them like each other?
  - You can't pick a VRM because of its size **pick it for its impedance**
  - Decoupling needs to be appropriate for the dynamic currents **and is specific to a PCB design**
- **Lack of Awareness** **The power supply is a common source of system issues**
  - Poor EVMs, Reference Designs, and Lack of Trade Studies **result in system issues**
  - Parts and EDUs often not available for testing before the final design pass **EM is Simulation needed**
  - Where are the resonances, what are the dynamic currents?
  - You almost always need an iteration

**It's easy to get right if you follow a few basic rules and**

**Measure - Model - Simulate - Measure**

# Example: Power to Core WCCA

## The Target Impedance Concept




Each power rail has an allowed voltage range to work with, often 5% of Vout, but can be smaller or larger. For example, a 2.5V power source suppling 1A, may have an allowed operating range of 5%...

$$\Delta V = 2.5V \cdot 5\% = \pm 125\text{mV}$$

From this allowed range, subtract the DC terms, ripple and PSRR to determine the Target Impedance. Some engineers BUDGET 1/3rd of the noise for dynamic current, which would reduce this to ± 42mV. Sensitive circuits that include PLLs, such as SERDES transceivers are often lower voltage and typically ± 20mV or less.

Assuming one resonant peak and excitation at the resonant peak frequency

$$Z_{\text{Target}} = \frac{(Power\_Supply\_Voltage) \times (Allowed\_Ripple)}{Current}$$

$$+2.5\text{V\_Target\_Impedance} = \frac{1}{3} \cdot \frac{2.5\text{V} \cdot 5\%}{1\text{A} \cdot 50\%} = 0.083\Omega$$

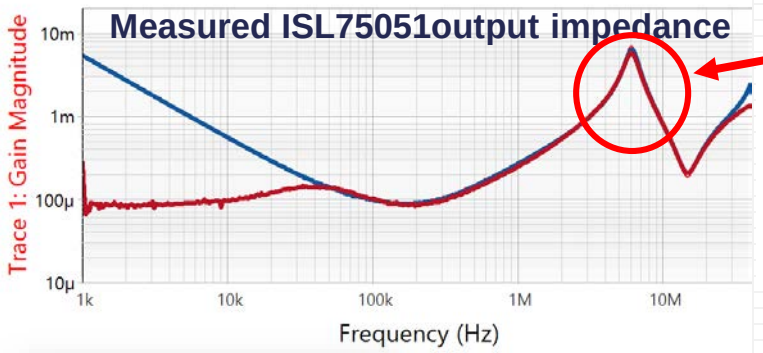
$$\text{BW(Trise)} = \frac{0.35}{\text{Trise}}$$

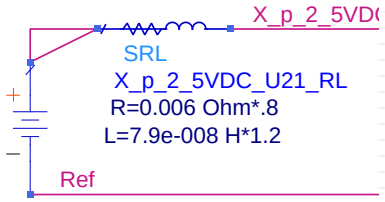
While the edge speed and dynamic current are unknown, a conservative BW limit was 300MHz in this case

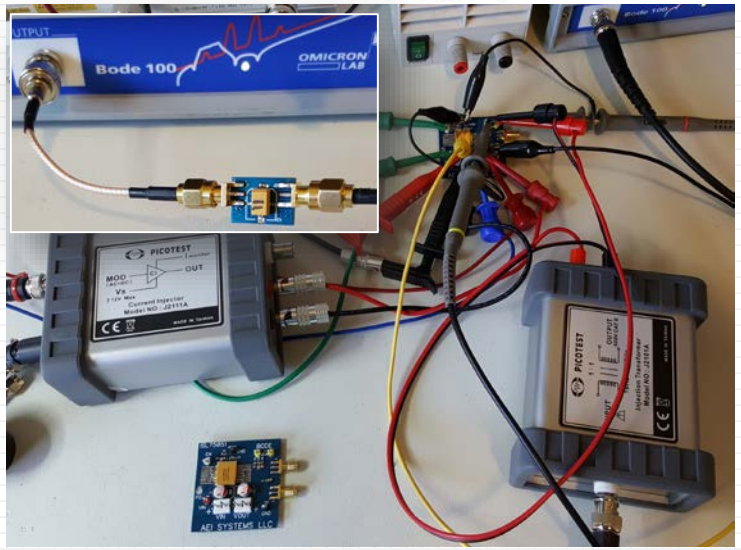
# Example: Power to Core WCCA

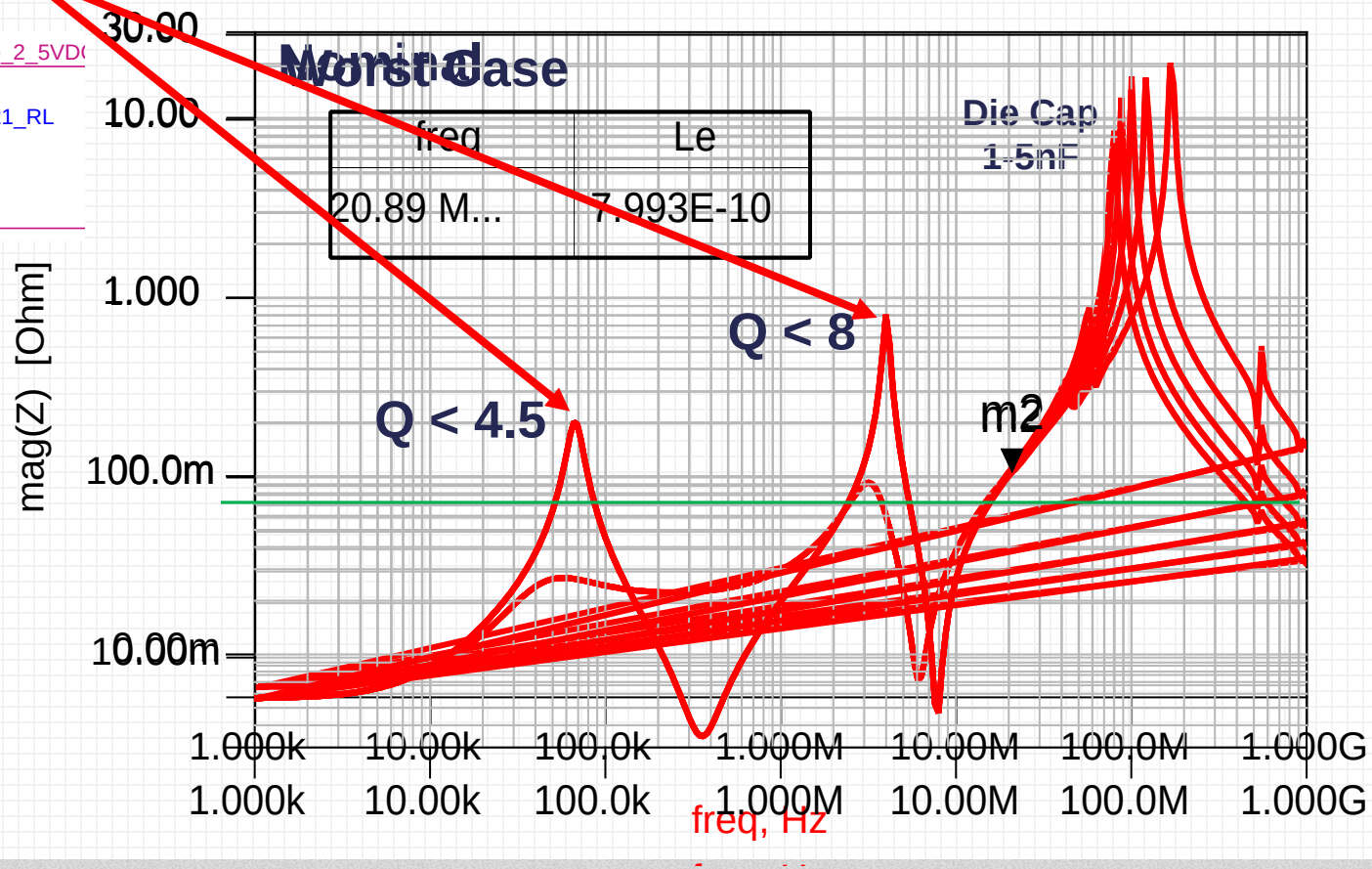
- **Compliance: Q < 2 and Impedance < 0.083Ω**

Improper capacitor selection

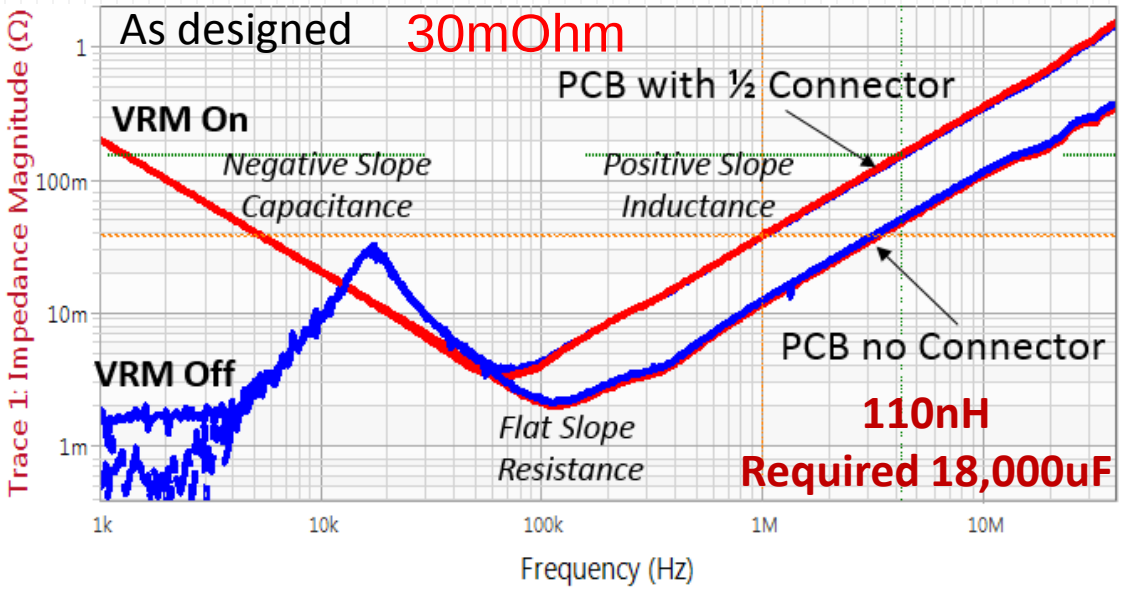


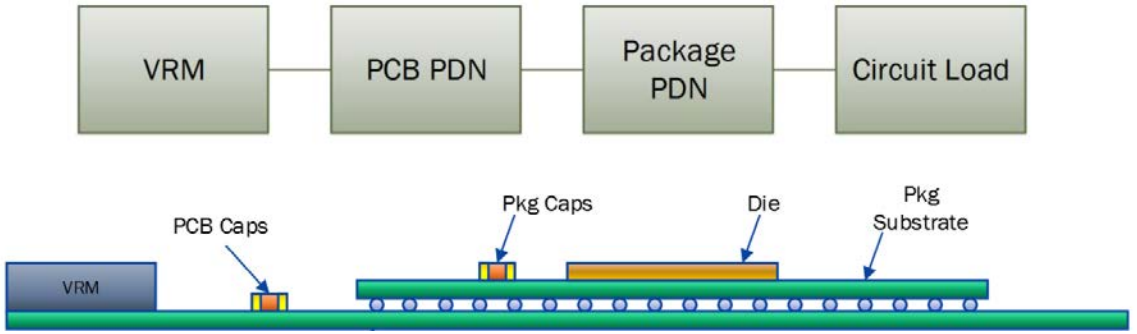



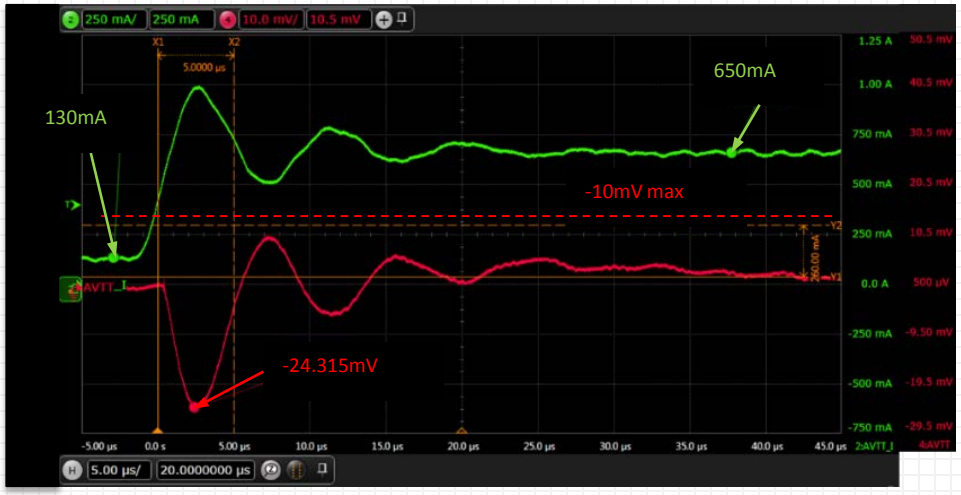



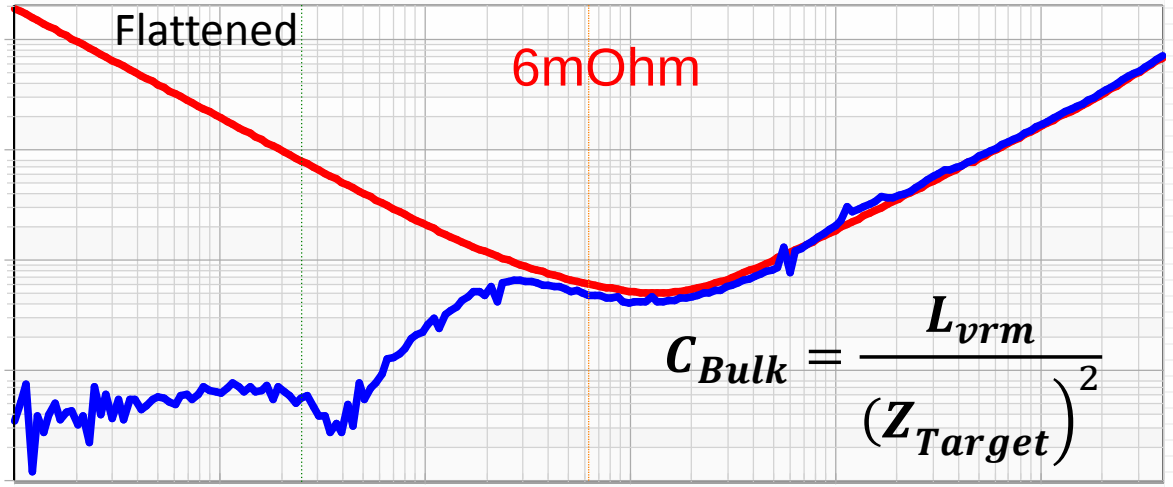
# Example: Power to 32Gb/s SERDES Transceiver




This “REFRENCE DESIGN” resulted in exceeding the allowed voltage deviation by 150% when powering just ONE of FIVE transceivers



# Example: Power to 32Gb/s SERDES Transceiver

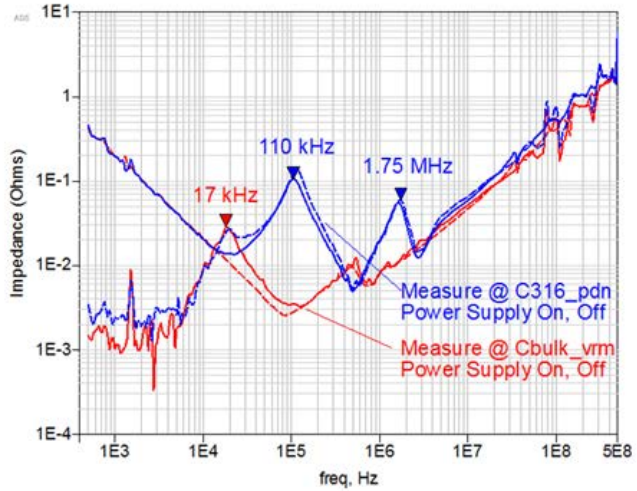
The 1.2V MGTVCC powers the transceivers. There are 10 total transceivers and each results in a 500mA step at turn on. At least one bank of 5 is required or 2.5amps, meaning that the Zo has to be < 4mΩ (2.5mΩ in order to account for WC)

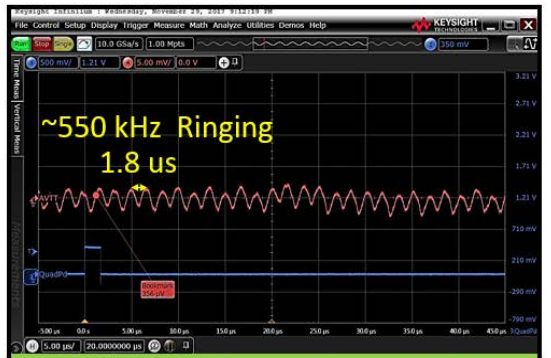
**The specialized D2Cap™ VRM controller has no compensation or linear control NO WAY TO FIX IT!**

**Measuring the excess inductance and solving for the capacitance requires 18,000uF to achieve the 10mV allowed transient.**

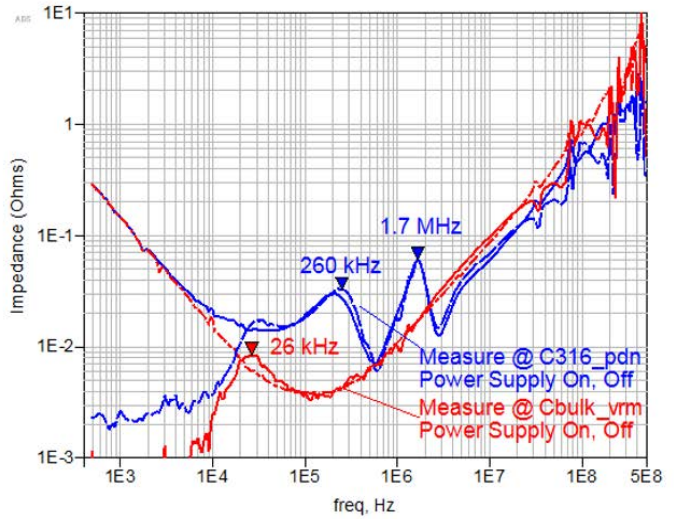
The switching frequency and output inductor were modified at the expense of efficiency. This reduced the required capacitance to 1200uF. **Note: due to 8nH inductance of the pins an additional 1300uF per pin we required after the connector.**


- Board with current sense wire loops
- VRM no Mods
- 1 Quad powered on



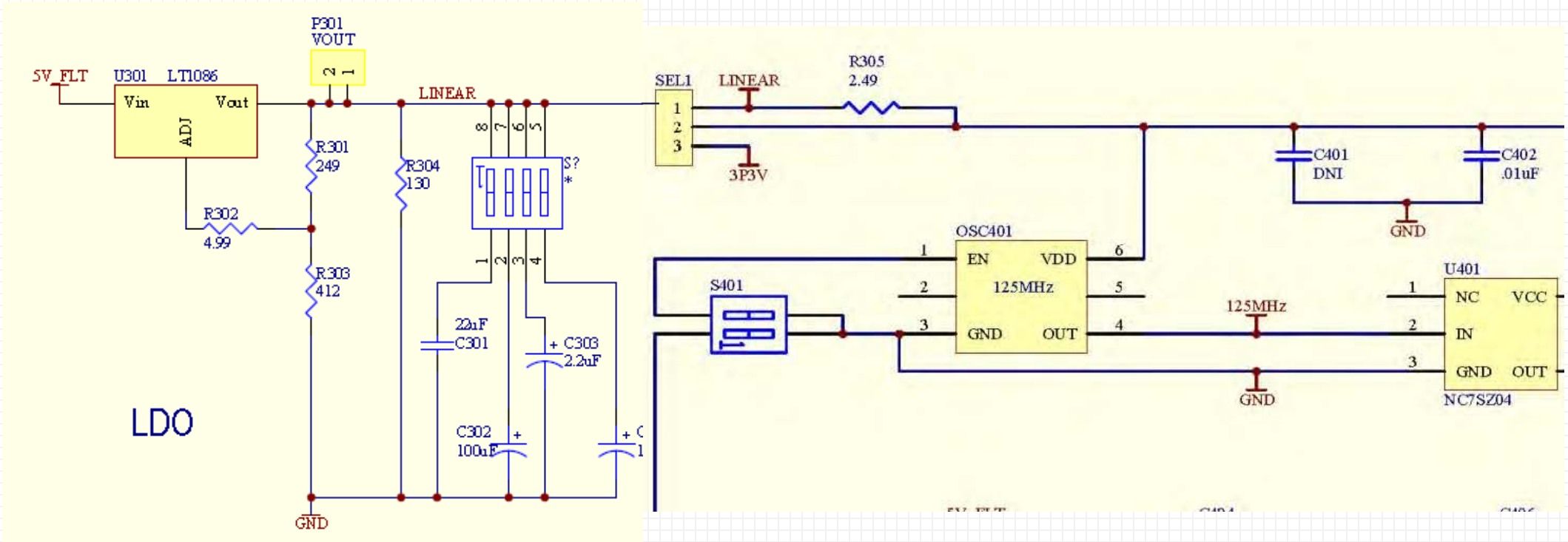




- Board without current sense wire loops
- VRM Modified
- Bulk Caps added
- 1 Quad powered on



# Example: Power Impact Clock Jitter

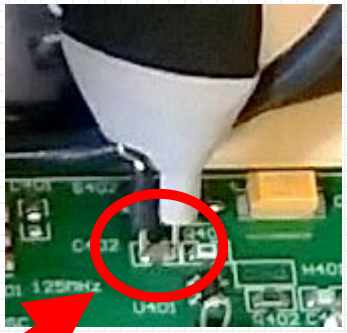
3.3V LDO various bulk capacitors
& 10nF Decoupling Cap



# Example: Power Impact Clock Jitter

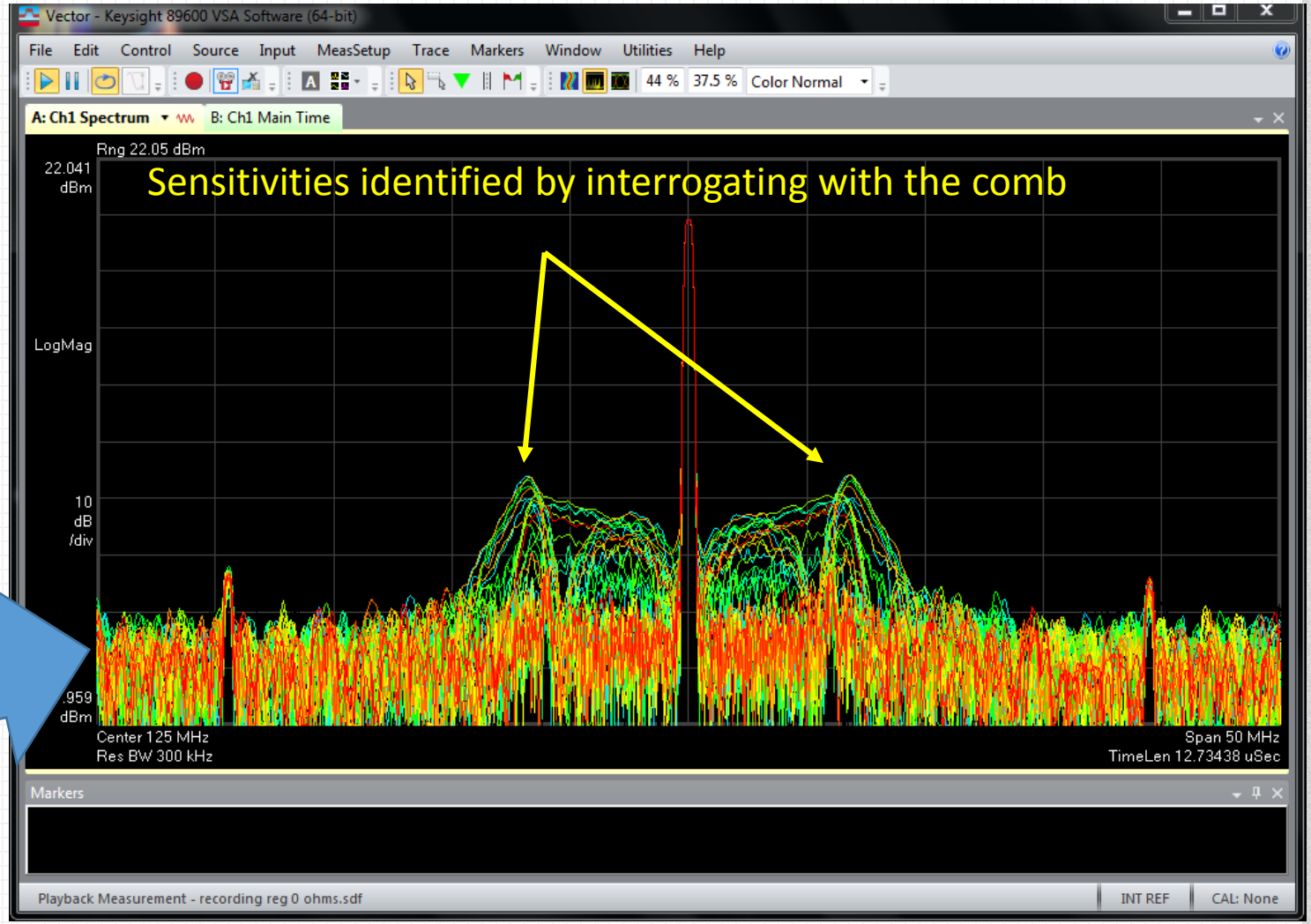
**Injecting the Harmonic Comb signal at the Clock capacitor shown earlier reveals the impedance resonance**


Clock and buffer



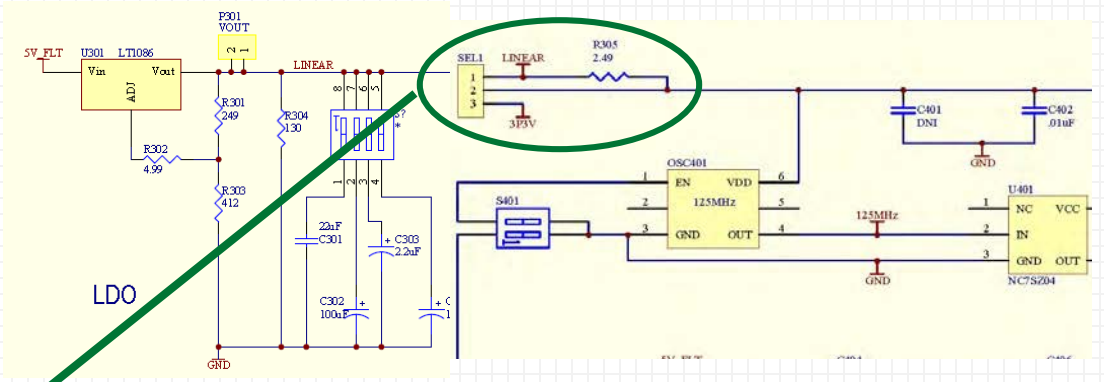
10nF cap

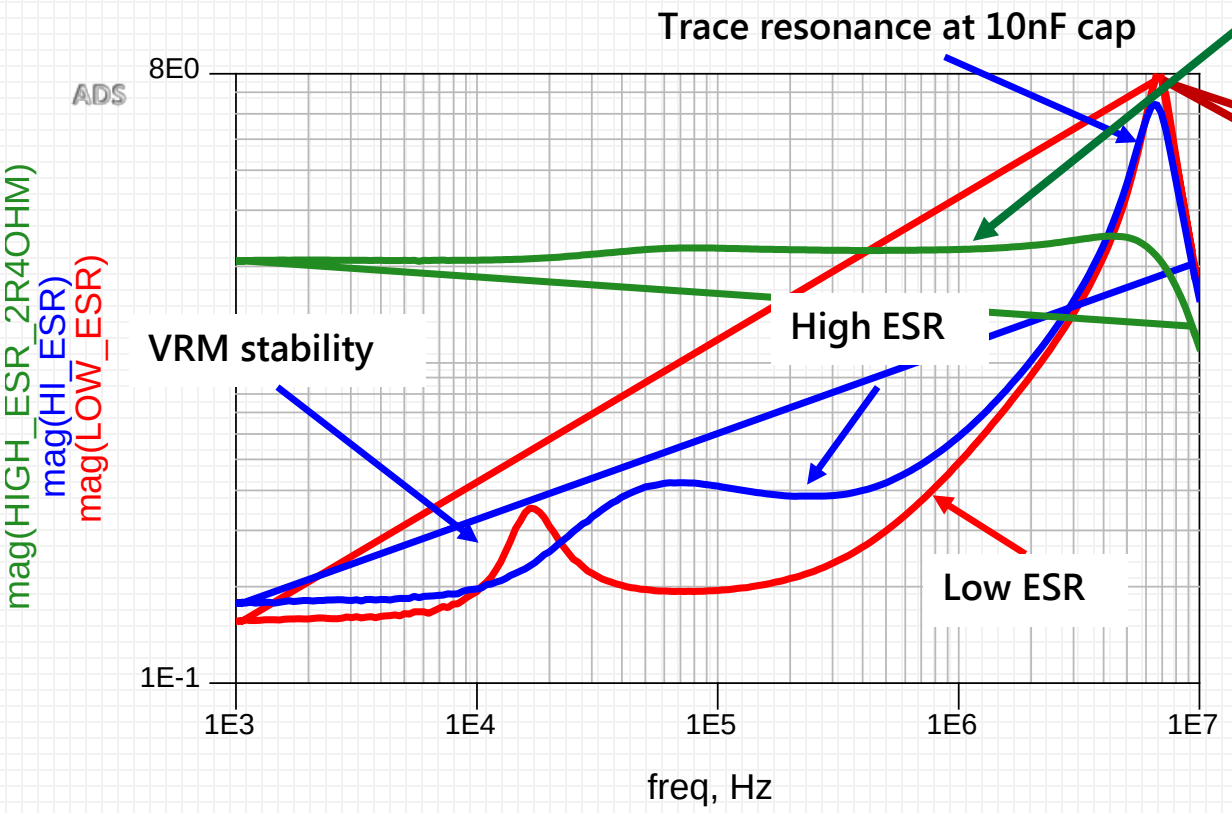
Clock output

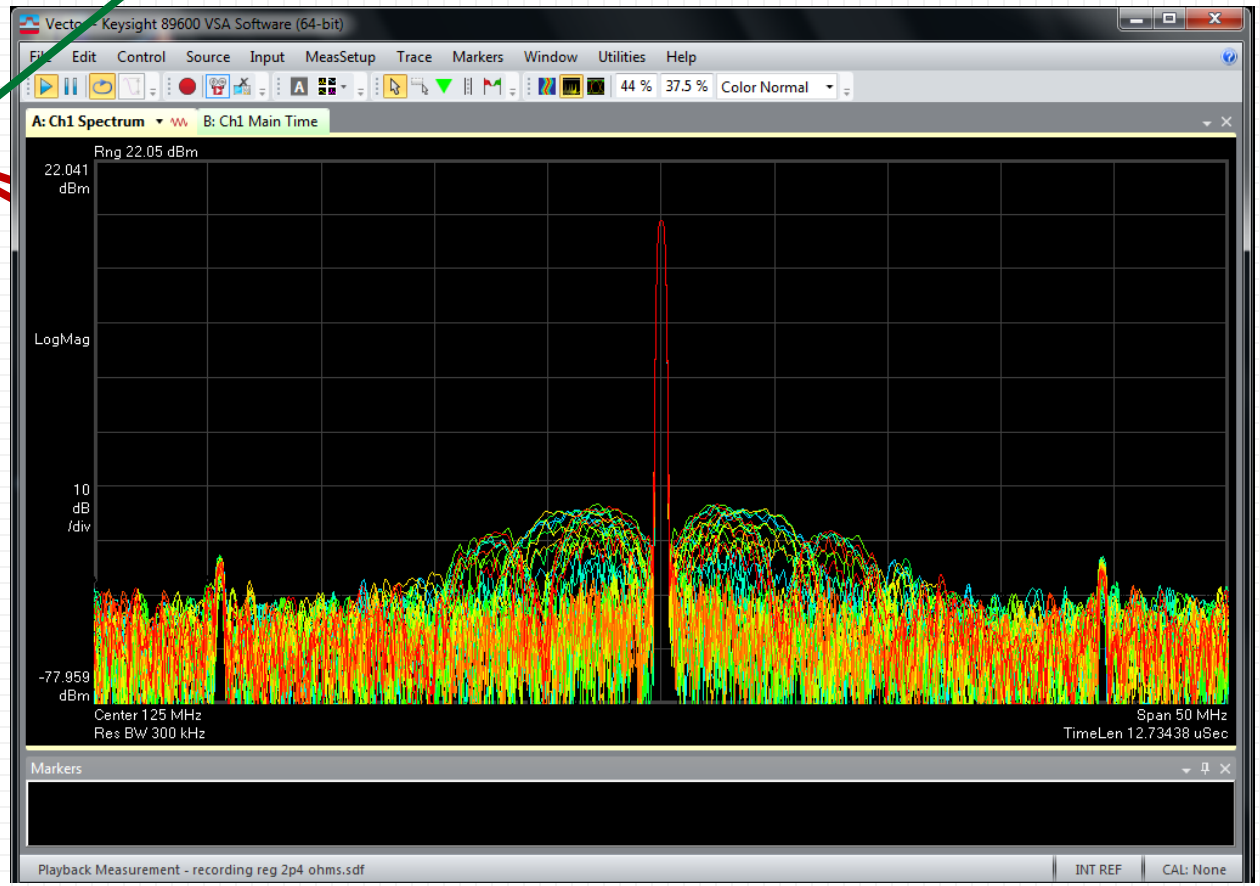


# Example: Power Impact Clock Jitter

Flattening the impedance eliminates the jitter



# YOU CAN'T TEST YOUR WAY OUT OF PI!!

- **PCB design / decoupling "rules-of-thumb" generally don't work well**
  - Involves trade-offs - the impact on resonances need to be weighed carefully
  - Should be based on Test Data
  - But measurements are often hard to perform – Lack of Access
- **A mismatched VRM exacerbates resonances**
  - Almost impossible to fix due to lack of controller ESR caps and board space
- **Tolerances make Qs much worse – give rise to rogue waves**
- **Simulation is challenging, time-consuming, and expensive**

# Lessons Learned

- **Power Integrity Matters to the Entire System**
  - Don’t ignore it, believe its trivial or irrelevant, or leave it until the end
- **Perform Measurements Prior to Selecting the VRM**
  - Select the RIGHT VRM, not the BEST VRM
- **Design for Flat Target Impedance**
- **Plan for Iterations/Board Spins *“Get it right the 2nd time”***

# References and Resources


1. **Ultra-Low Impedance Measurements Using 2-Port Measurements**
   http://literature.cdn.keysight.com/litweb/pdf/5989-5935EN.pdf
2. **PCB Characteristics Affect PDN Performance,**
   http://www.edn.com/design/pc-board/4429719/PCB-characteristics-affect-PDN-performance
3. **The Inductive Nature of Voltage Control Loops,**
   https://www.edn.com/electronics-blogs/impedance-measurement-rescues/4438578/The-inductive-nature-of-voltage-control-loops
4. **A 5-V Input, 1.6-A Output, Non-Synchronous Buck Converter**
   http://www.ti.com/lit/ug/slvu153/slvu153.pdf
5. **Power Integrity For 32 Gb/S Serdes Transceivers, Heidi Barnes, Jack Carrel, Steve Sandler, Designcon 2018**
   http://schedule.designcon.com/session/power-integrity-for-32-gbs-serdes-transceivers/851162
6. **Top Three EMI and Power Integrity Problems with On-Board DC-DC Converters and LDO Regulators**
   https://interferencetechnology.com/top-three-emi-power-integrity-problems-board-dc-dc-converters-ldo-regulators/#


- **AEi Systems Power Integrity Publications**
  - https://www.aeng.com/power_integrity.htm
- **How to Design for Power Integrity YouTube Video Series**
  - https://www.youtube.com/playlist?list=PLtq84kH8xZ9FNXAsf-odoGNe6h5A6D3in
- **SI & PI Resources from Keysight EEsof EDA**
  - https://www.keysight.com/main/editorial.jspx?cc=US&lc=eng&ckey=2658533&nid=-11143.0.00&id=2658533
- **Power Integrity Book: Measuring, Optimizing, and Troubleshooting Power Related Parameters in Electronics Systems**