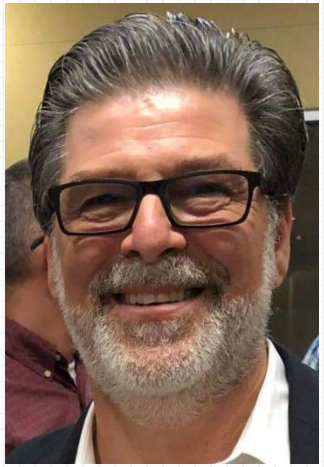
Power Integrity Challenges In the Space Industry, An Update

presented by:
Steve Sandler of AEi Systems and Picotest

ANALYTICAL HEAVY LIFTING

PICOTEST

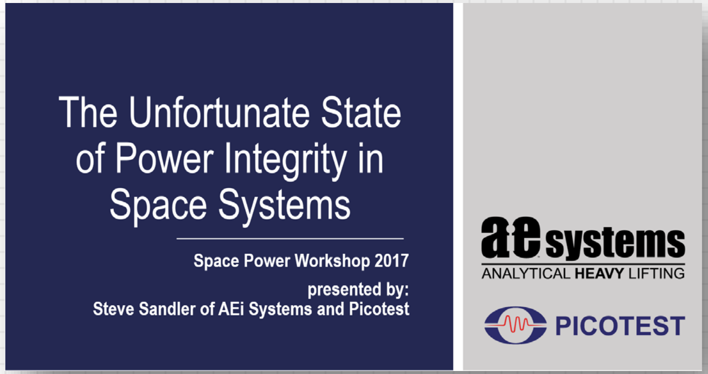
Bio



- Steve Sandler has been involved with power system engineering for more than 40 years.
- Founded AEi Systems, a well-established leader in worst case circuit analysis and troubleshooting of high reliability systems
- Founded PICOTEST.com, a company specializing in power integrity solutions including measurement products, services and training.
- Frequent lecturer and author of articles, peer journals and power related books and of course a regular presenter at Space Power Workshop.
- GPS Satellite – Rubidium and Cesium clock system design support and analysis
- International Space Station - system design support and analysis
- LHC Accelerator at CERN - system design/troubleshooting support and analysis

In 2017 we called it an Unfortunate State

- **Design is still compartmentalized – PS Designers – Board Designers – Load Designer**
- **Semiconductor manufacturers could and need to do much more**
  - VRM data are usually poor, wrong, or non-existent
  - EVMs often poorly designed – 'Proprietary' data precludes usability
  - Models are often poor – Inaccessible for tolerances or non-existent
  - Part stability is often poor – Guidance limited
- **MUST take your own data (Output Impedance, PSRR)**
- **Dynamic currents are often unknown**
- **Board layout and decoupling must be simulated/optimized together with the VRM to achieve flat PDN impedance**



The state is "Unfortunate" indeed – program delays, cost overruns, unreliable hardware

We are encountering this on <u>EVERY single project</u>.

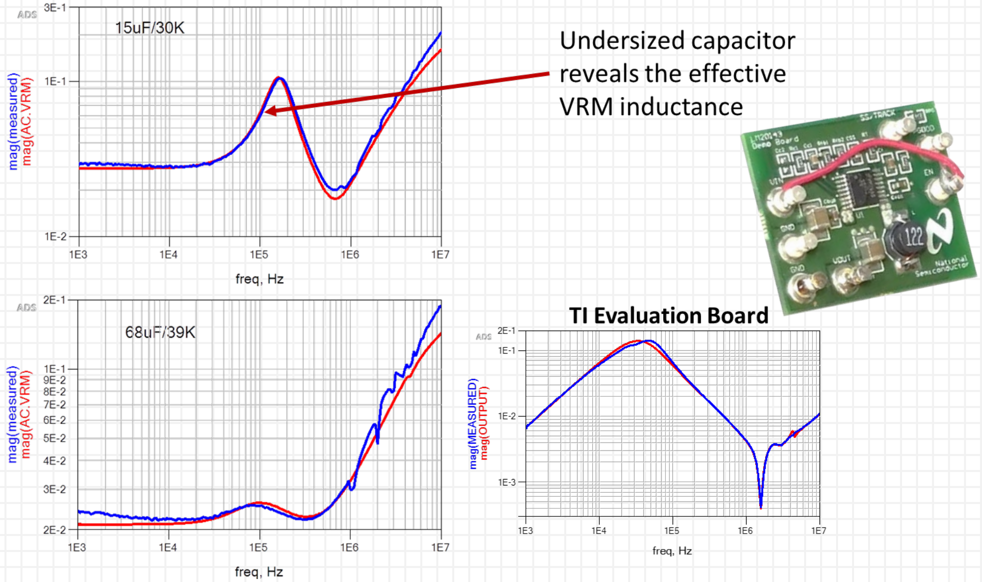
Its pervasive and the awareness of PI needs to be raised

Score Card 2021 – Still Failing

- **EVMs Still Poor/Data Still Unavailable**
  - EVMs not flat impedance design, not vetted well
  - Testing a challenge
  - Power IC impedance is not being measured, reported, or correlated – Need to get your own data
- **Poor Models Still Prevalent**
  - Models are still not accurate – 1st order at best - Linear regulators are the worst
  - Model operation, features, structure, characteristics not documented
    - **WC tolerances are not defined or documented**
  - Power sequencing - Stability are not supported well
- **PDN Impedance - Still No Plan for Power Integrity**
  - Target impedance requirements are still undefined
  - Failing recommended operating voltage ranges WC EOL
  - Poor recommendations and EOL tolerances lead to non-compliant designs
    - **Suggestions are inadequate - lead designers astray**
  - Not including the PCB in simulations

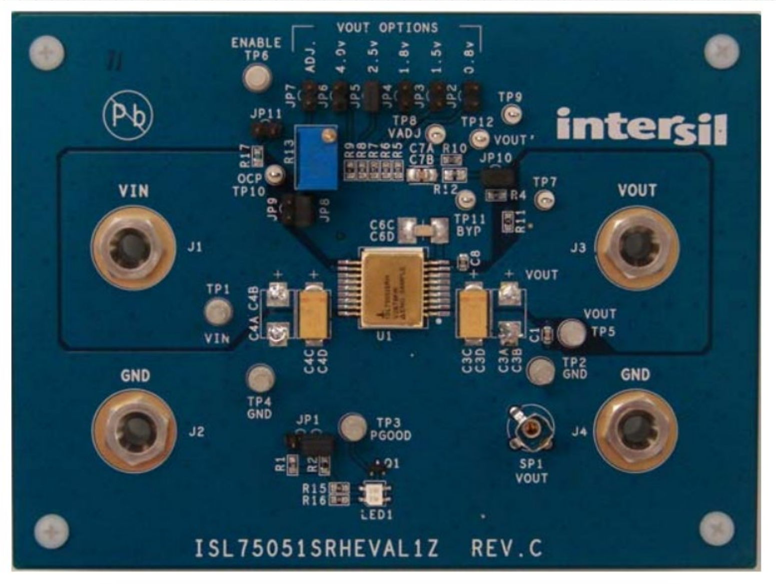
EVM’s Still Poor

- Often not testable
- Board files not supplied
- Connectors impact measurement
- Tough to solder
- Recommendations not vetted for WC
- Do not support Power Integrity

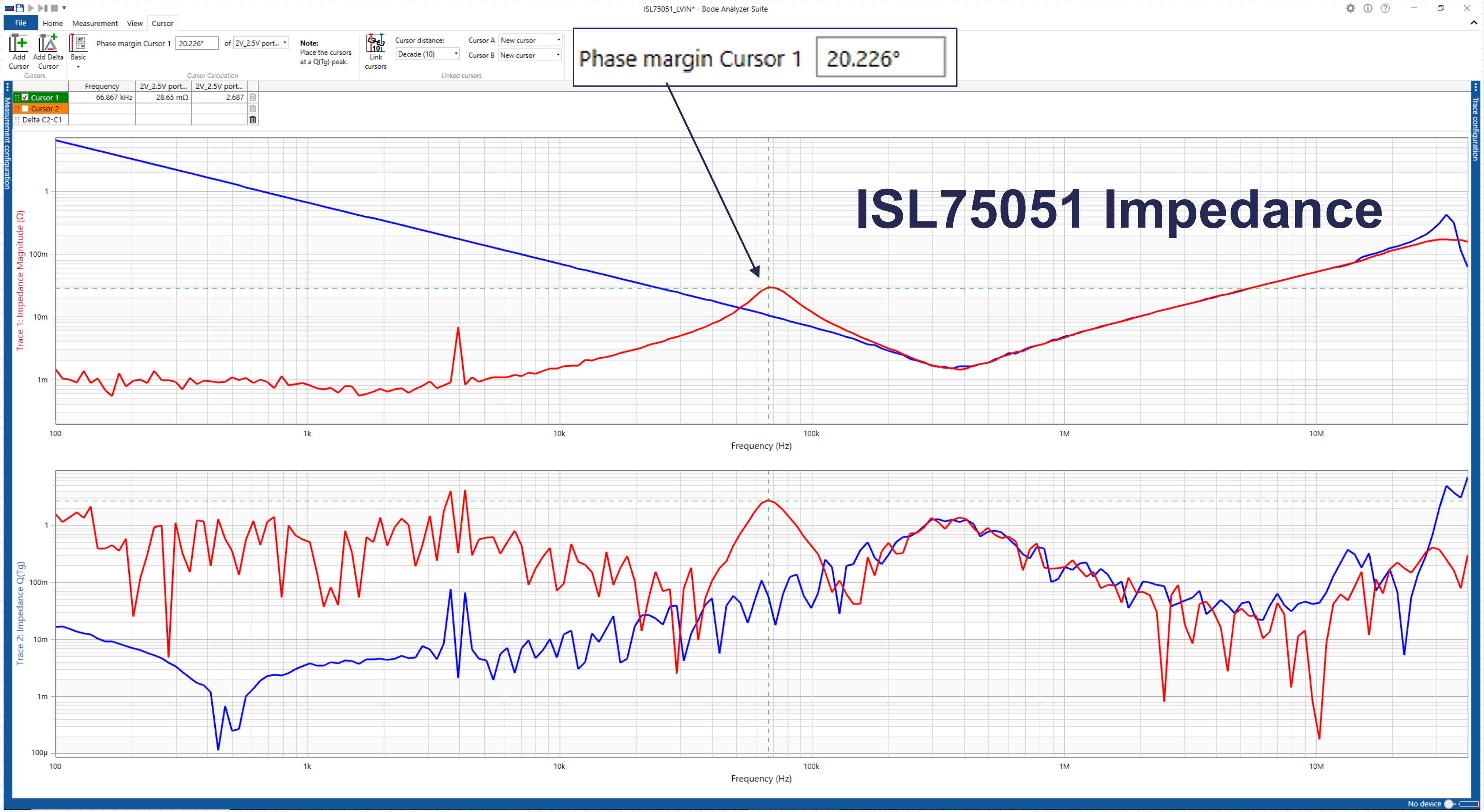


In general, EVMs are not designed for flat impedance

(But easily could be)



Get Your Own Data – What We've Done

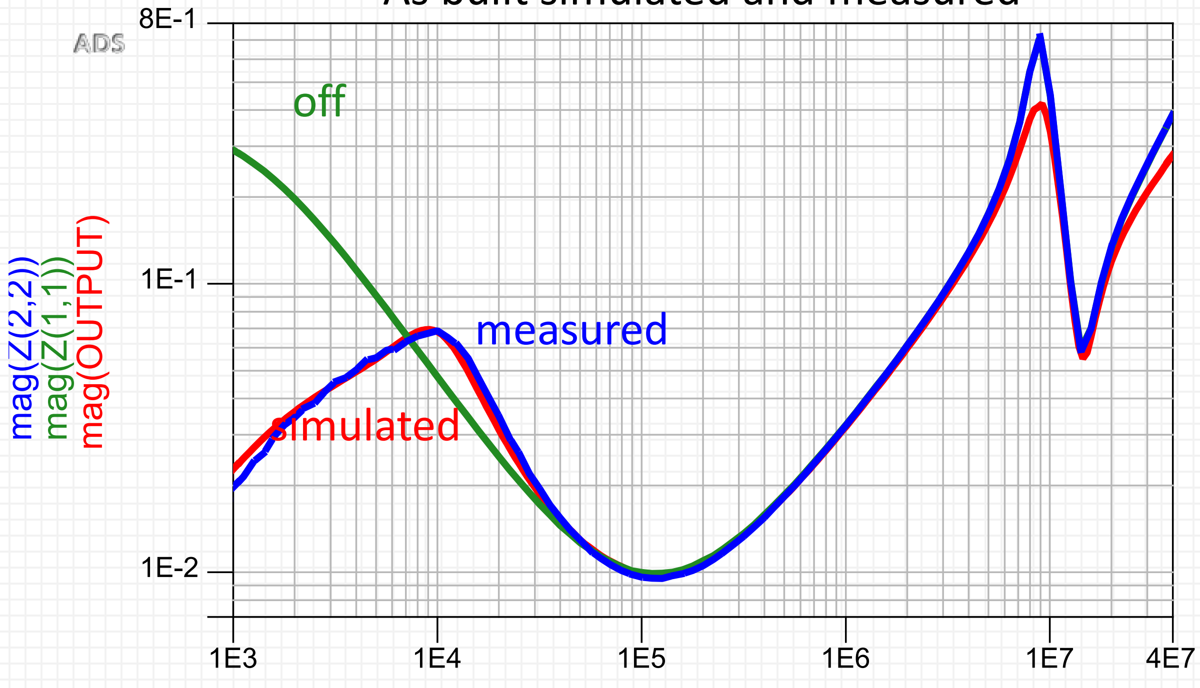


TPS50601 EVAL Board

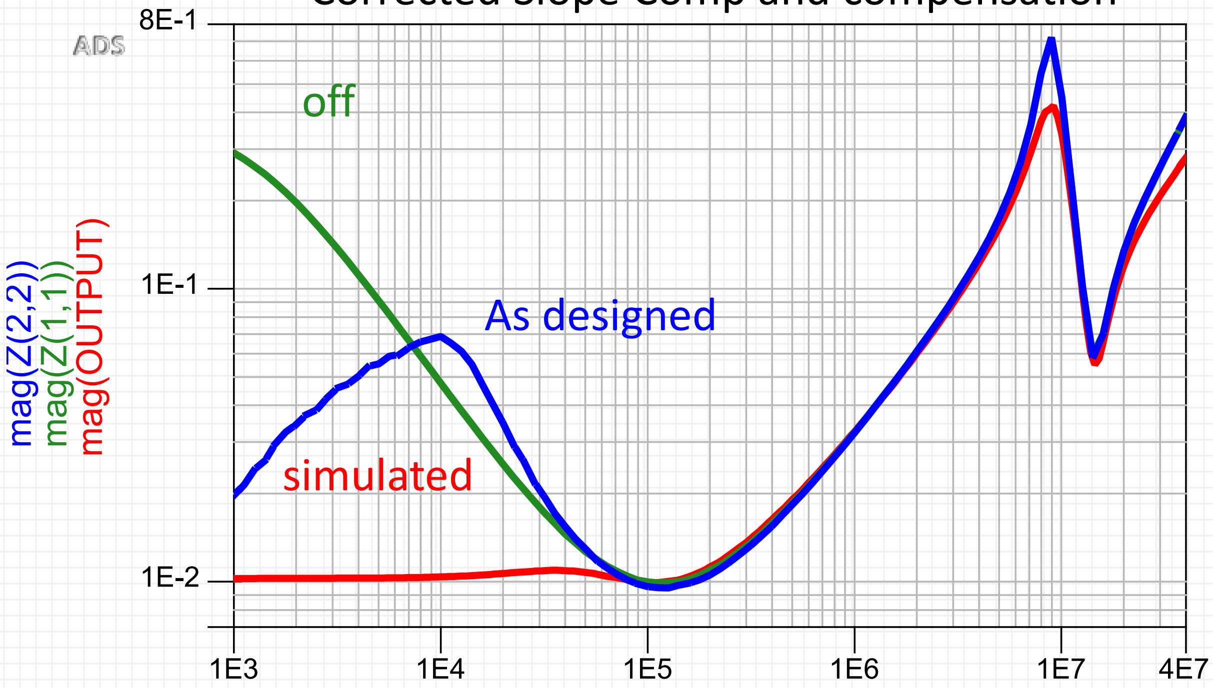
What we measured as part of this effort

- Vc vs load current (to determine Ri or power stage transconductance
- Bode plot (for correlation with the model)
- Modulator gain (for correlation and slope comp determination)
- PSRR (for correlation and slope comp determination)
- Output impedance (for correlation and Ri determination)
- Switch waveforms
- Ripple for correlation pictures

As built simulated and measured

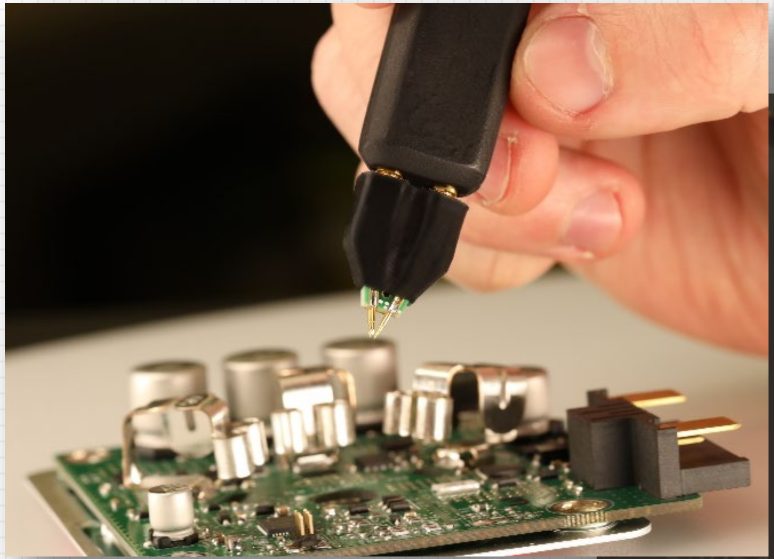


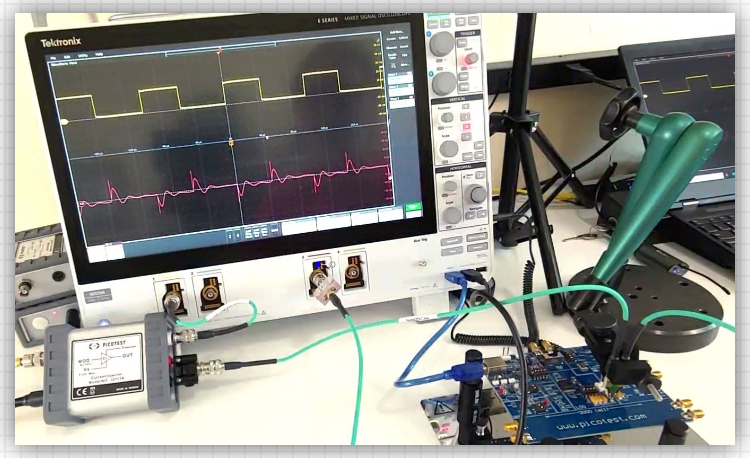
Corrected Slope Comp and compensation

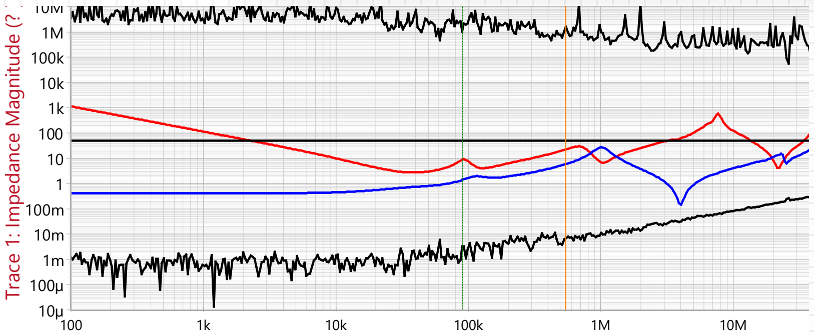


New 2-port Probes Helps with PDN Test

- **Impedance characterization is essential and not happening**
- **Vendors leave out the data you need**
- **Often dozens of rails**
  - Lower voltages
  - Higher and more dynamic currents
  - These drive the need to measure impedance
- **New test tools help in the model models creation and measurement**
  - Picotest P2102A 2-Port Probe
  - Transient Step Load testing or Impedance





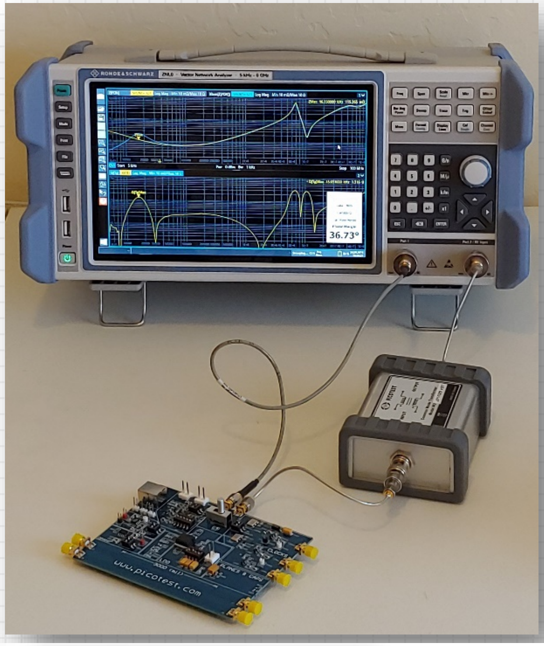


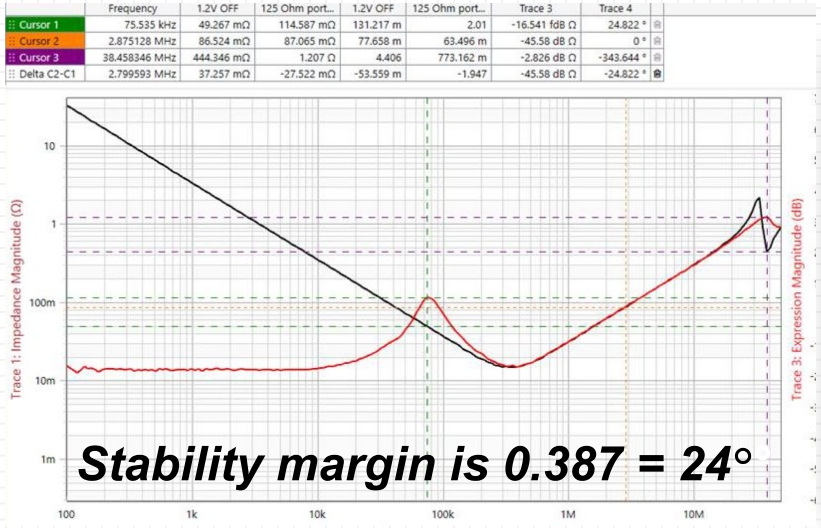
Stability Issues -- What We've Done

- **We've created a method of assessment that doesn't require access to the control loop, includes stability margin and works for multiple control loops (NISM)**
  - We've taught how to solve most stability issues with just one measurement
- **We've brought stability measurements to oscilloscopes making the measurement even more accessible**
- **We've taught how to get the data required from measurements (measurement-based modeling)**

NISM – Stability via Output Impedance

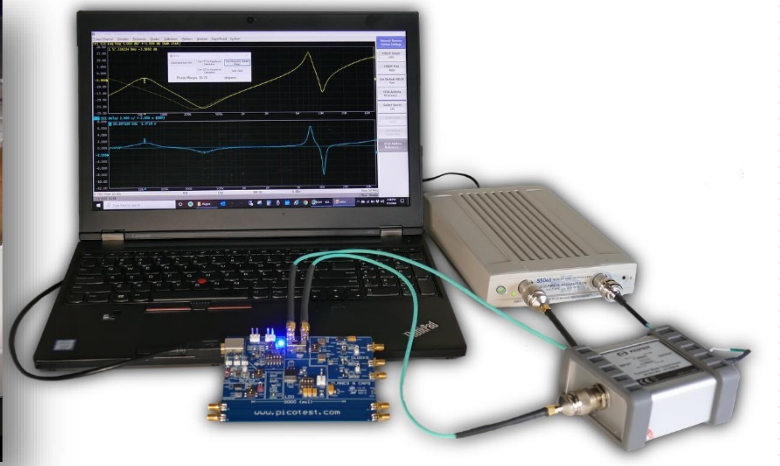
- Now in multiple VNAs
- OMICRON Lab Bode 100 – Low Cost
- Keysight E5061B
- Copper Mountain Compact VNAs
- Rohde & Schwarz ZNL





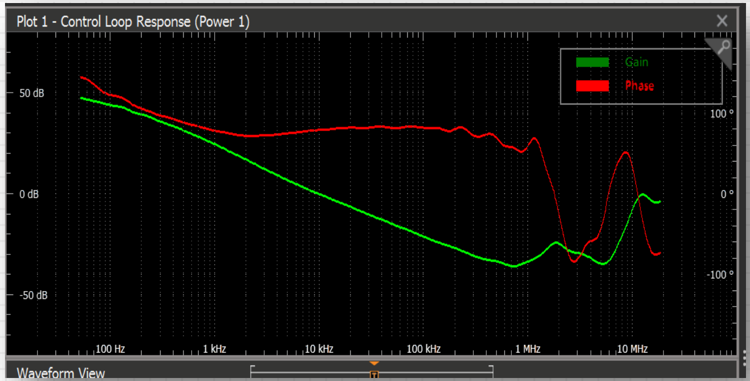
	Frequency	1.2V OFF	125 Ohm port...	1.2V OFF	125 Ohm port...	Trace 3	Trace 4
Cursor 1	75.535 kHz	49.267 mΩ	114.587 mΩ	131.217 m	2.01	-16.541 fdB Ω	24.822 °
Cursor 2	2.875128 MHz	86.524 mΩ	87.065 mΩ	77.658 m	63.496 m	-45.58 dB Ω	0 °
Cursor 3	38.458346 MHz	444.346 mΩ	1.207 Ω	4.406	773.162 m	-2.826 dB Ω	-343.644 °
Delta C2-C1	2.799593 MHz	37.257 mΩ	-27.522 mΩ	-53.559 m	-1.947	-45.58 dB Ω	-24.822 °

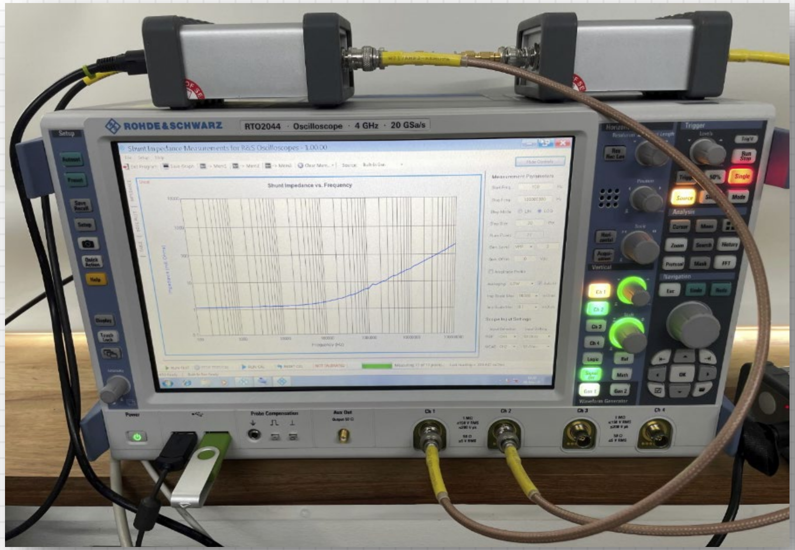
Stability margin is 0.387 = 24°



VNA Features in a Scope

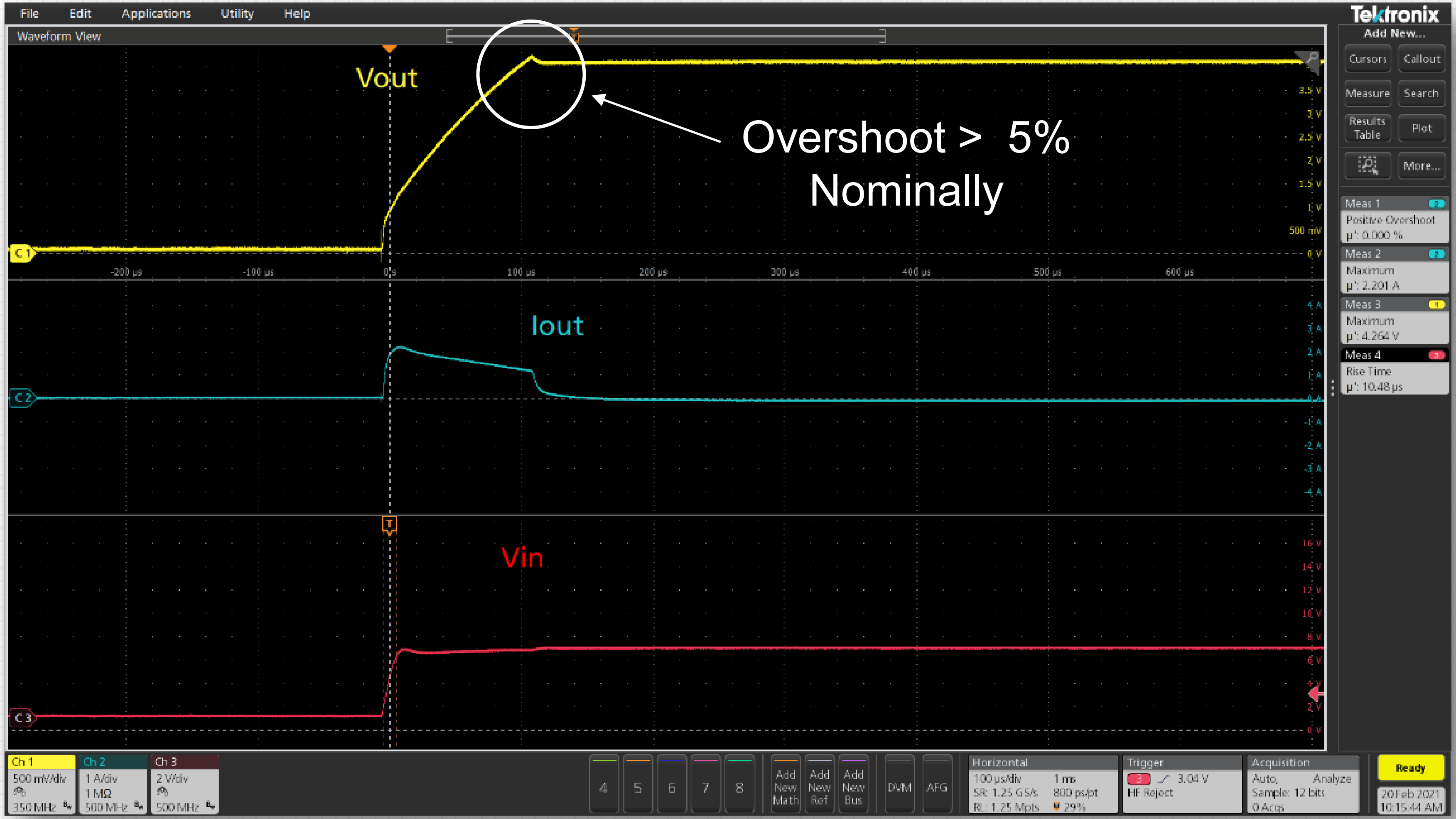
- What you can now do on a scope
- Milliohm Impedance Characterization
- Frequency Domain 10Hz to 250MHz
- Bode Plots / PSRR
- Negative Resistance
- VNA Features





Other Data Fires We are Routinely Fighting

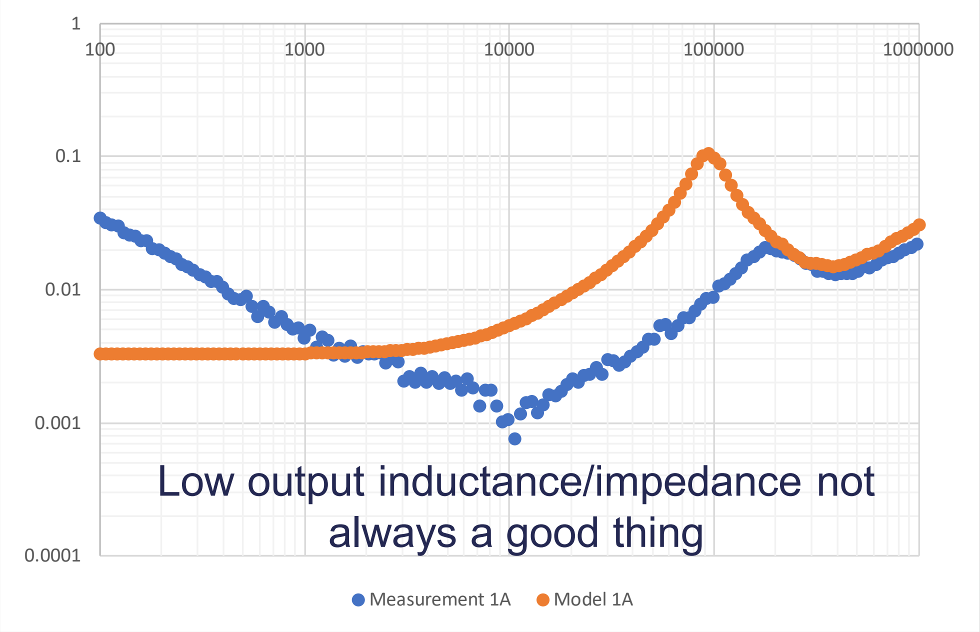
- **Short circuit – SET performance (no data, modeling challenging)**
  - Don’t know the maximum current the device will have during a short
  - Don’t know if the current limit is active. Makes limiting SET excursions challenging

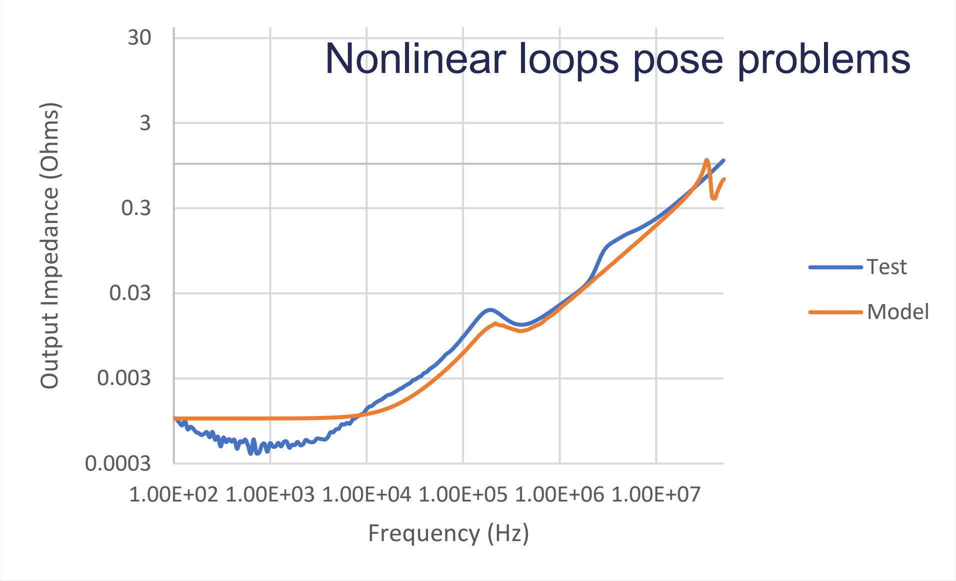


Poor Models

- **ISL75051A - Lack of model correlation at low voltages (<2.0V)**
  - Low current stability showed non-linear variations
    - **High bandwidth, large pole-zero variances**
  - High current performance shows inner loop poor stability
  - Low output inductance makes PCB inclusion important to prediction
- **Telecon held with Renesas**
  - Bode plots provided from foundry model
  - Concerns confirmed
- **Simplis is not the answer**
  - Intersil moved to Simplis for some POL models
  - Problem is if you have a POL feeding an LDO you can't simulate the LDO in Simplis so you still need 2 simulators AND you can do power sequencing!!

Test Condition	Test Resistance (Ohms)	Test Inductance (nH)	Model Resistance (Ohms)	Model Inductance (H)
125 Ohm port	15.42m	9.45E+01	16.44m	6.12E+01
125 Ohm port + 25mA	5.14m	3.31E+01	5.33m	3.23E+01
125 Ohm port + 50mA	3.58m	2.54E+01	3.50m	2.50E+01
125 Ohm port + 75mA	2.90m	2.23E+01	2.74m	1.94E+01
250mA	1.32m	1.32E+01	1.55m	1.16E+01
1A	1.23m	1.16E+01	1.09m	1.00E+01
2A	1.67m	1.16E+01	1.02m	1.02E+01
3A	1.16m	1.51E+01	993u	1.02E+01

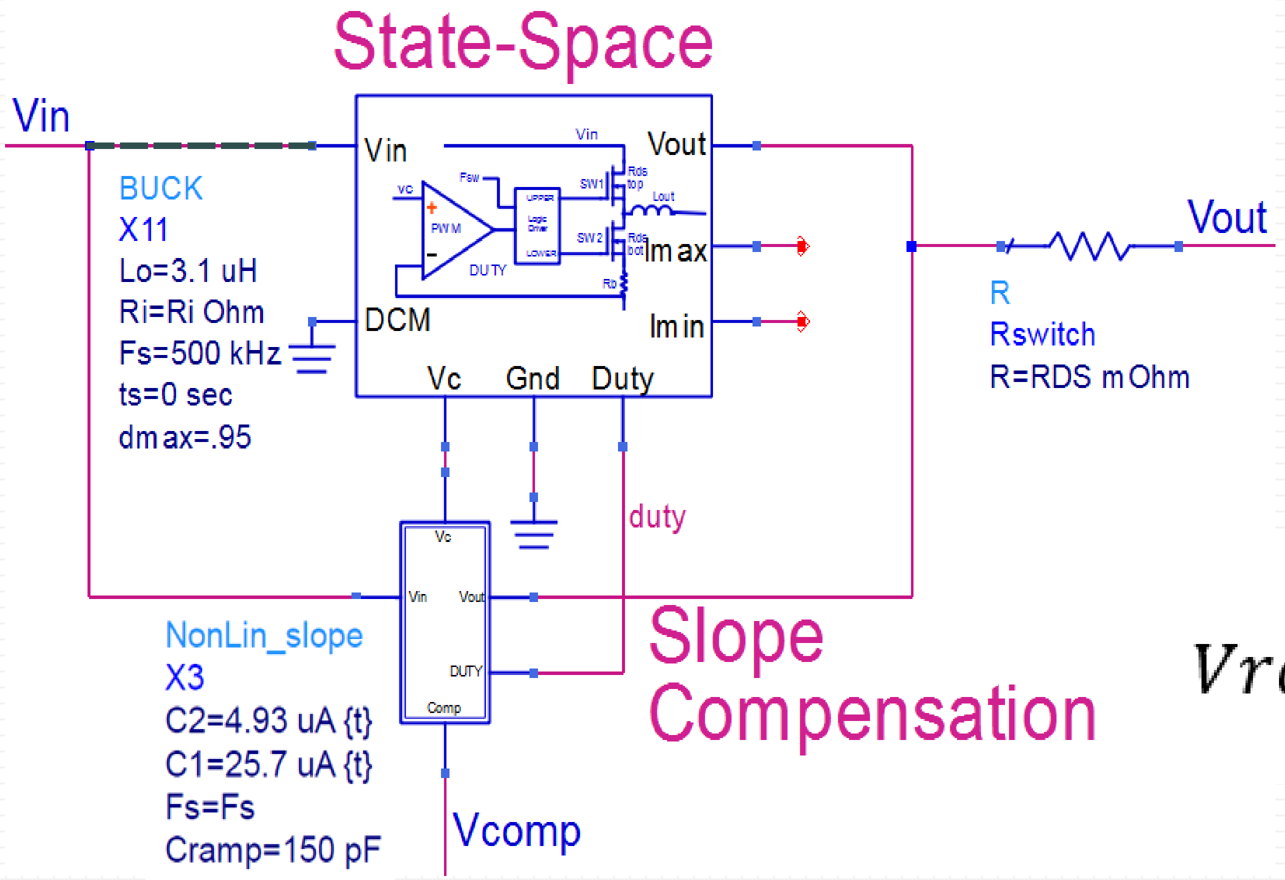




Poor Models -- What We've Done

- Create our own EVMs – Get the data
- Create our own models
- Published switching converter template created
  - Measurements defined
- Many correlated models can be found in the AEi System Power IC Model Library for PSpice

Measurement Based State-Space Averaged VRM Model

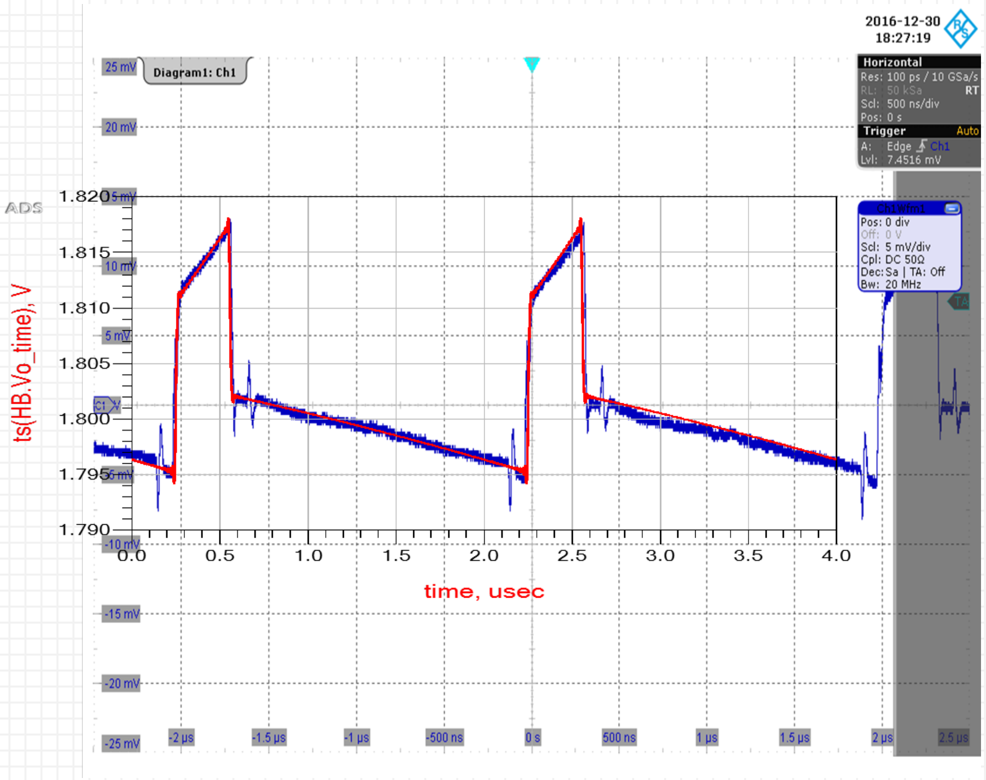


$$Vramp = \frac{C1+C2\cdot(Vin-Vout)}{Fs\cdot Cramp}\cdot DUTY$$

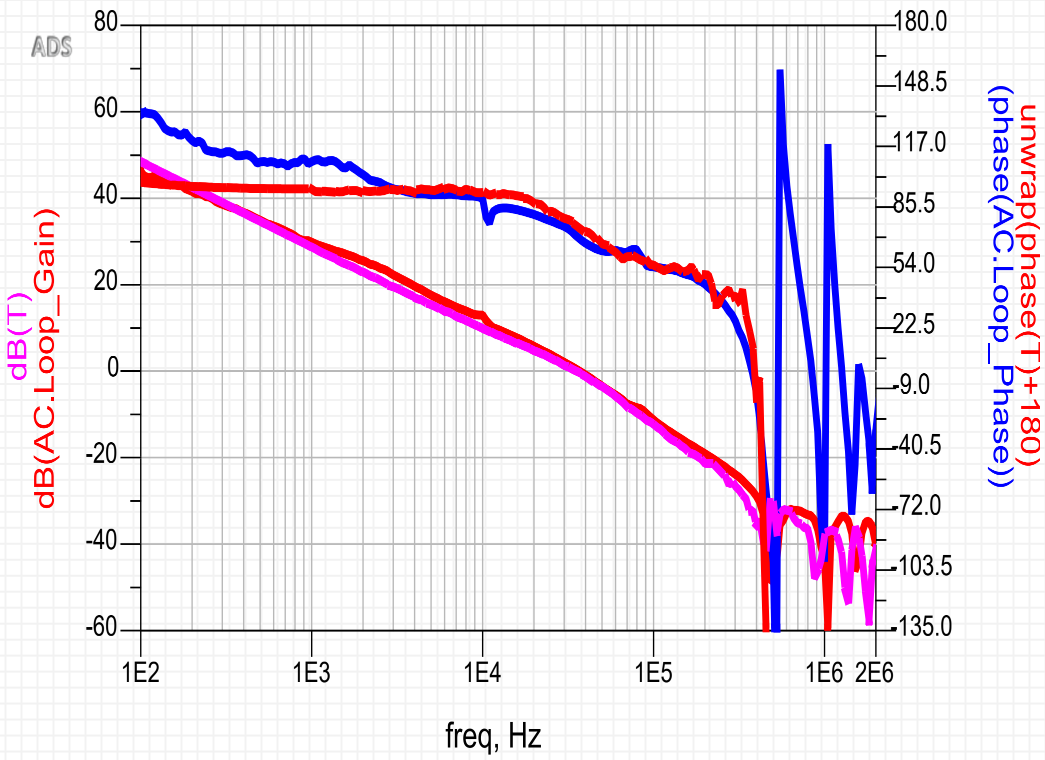
Measured vs Modeled

Large Signal Transient Ripple and Small Signal Gain/Phase

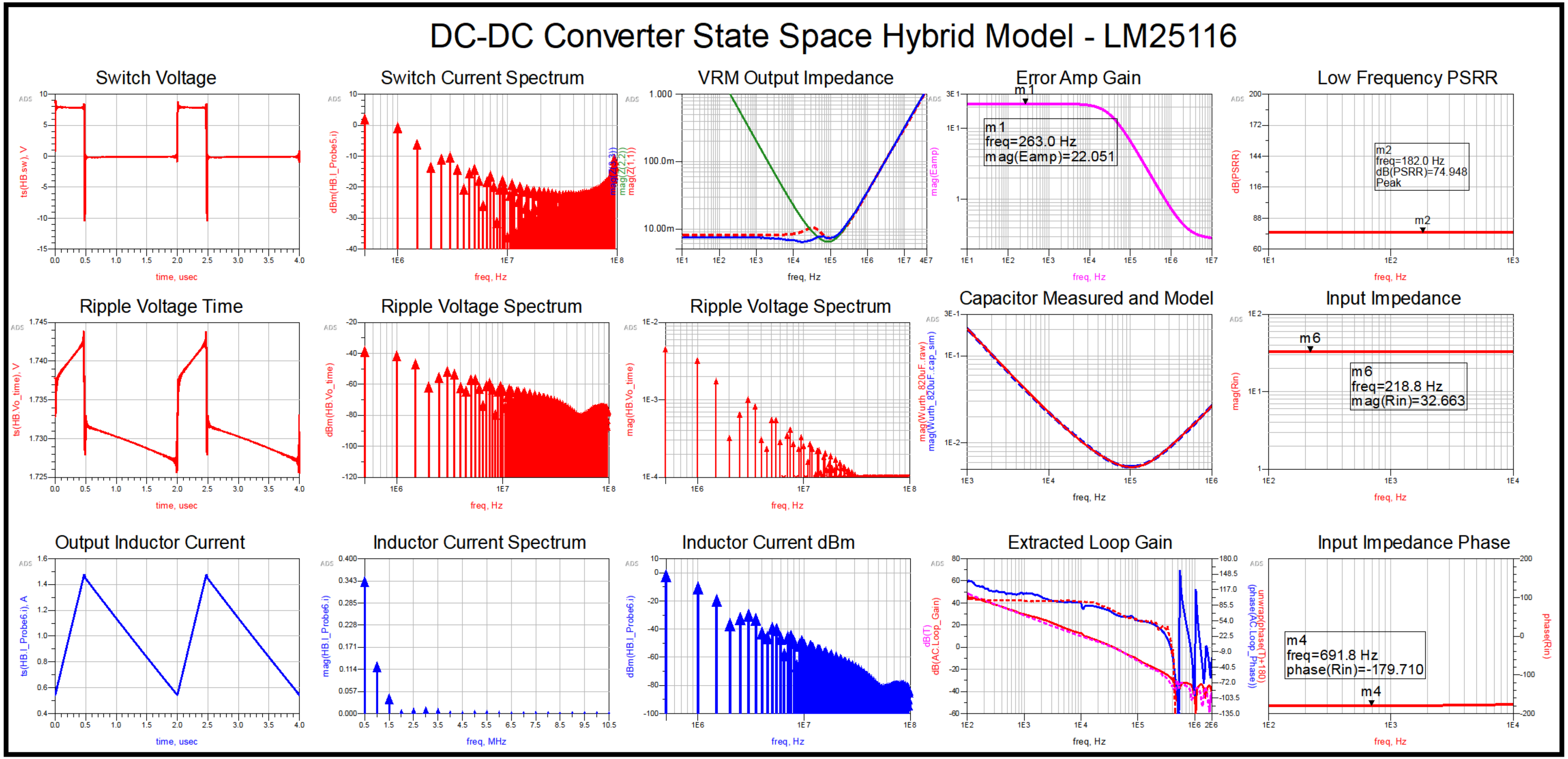
Time Domain



Frequency Domain



Full Time and AC Model Simulation



PDN Impedance Issues -- What We've Done

- We've created online classes teaching impedance measurement methods
- We've developed products, including probes that make it simpler
- We've published application notes and articles as well as presenting conference papers and "bootcamps"

MASTER THE FUNDAMENTALS OF POWER INTEGRITY AND POWER SUPPLY TESTING

Technical Session
October 20: SI/PI

A Holistic Power Integrity Approach Reduces Board Spins, Supports System Analysis and Reduces VRM Modeling Effort

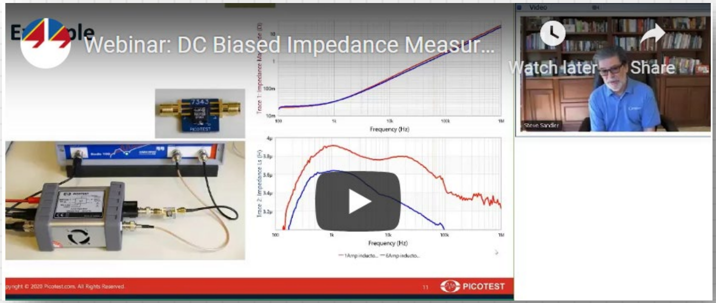
EDI CON Online 2019: Characterizing the VRM

Webinar: Power Integrity: Challenges, Best Practices, and Test Solutions for Sensitive Electronic Designs

Best Practices for Interpreting Power Integrity Measurements

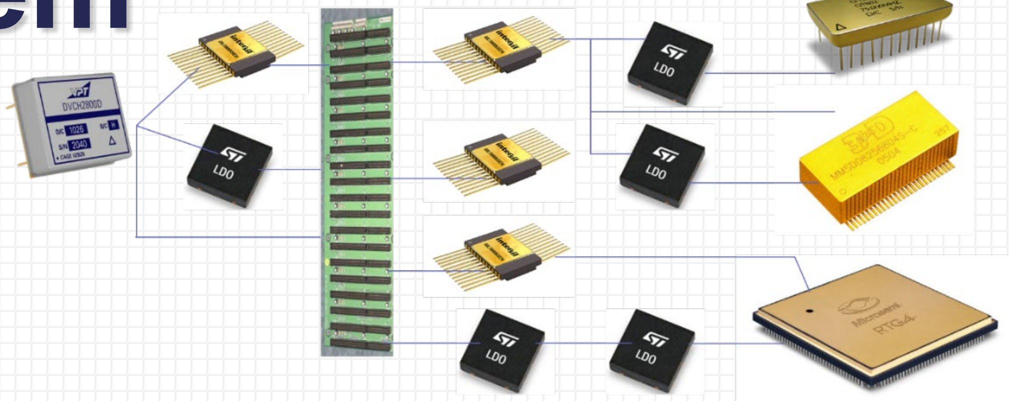
Measuring and Interpreting Impedance Data

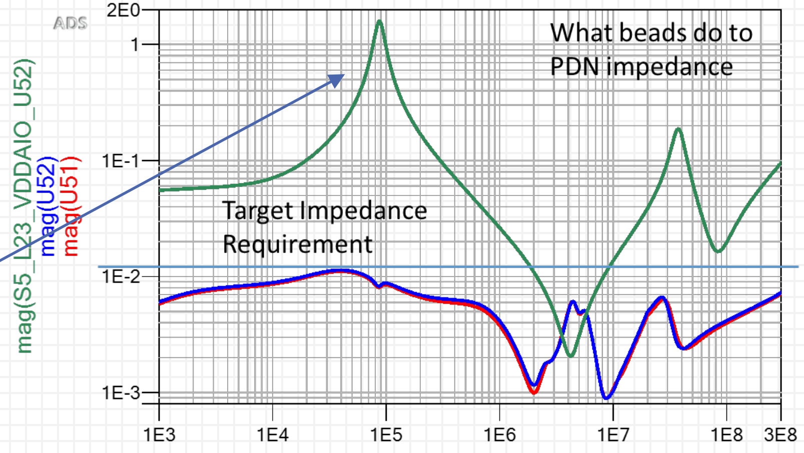
Webinar: VNA Impedance Measurement for Power Distribution Networks



Power Distribution System

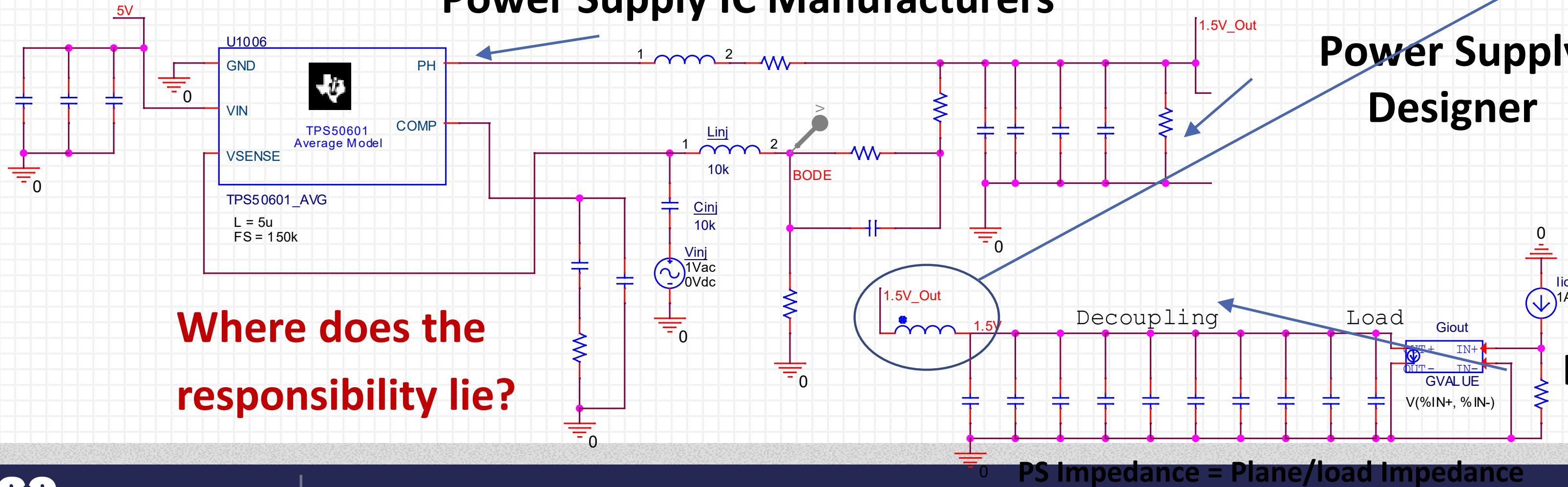
- **MEASURE - MODEL - ANALYZE – BUILD - TEST - ANALYZE – BUILD**
  - **Sorry if you thought it was TEST → BUILD → SHIP**
- **Design Still Compartmentalized**
- **PDN (Power Distribution Network) characteristics need to be assessed WC EOL via analysis**
  - Regulation, But Impedance → Drives Step load Excursions
  - Power Sequencing - Startup Overshoot – Shutdown
- **Bad design recommendations destroy the PDN impedance**





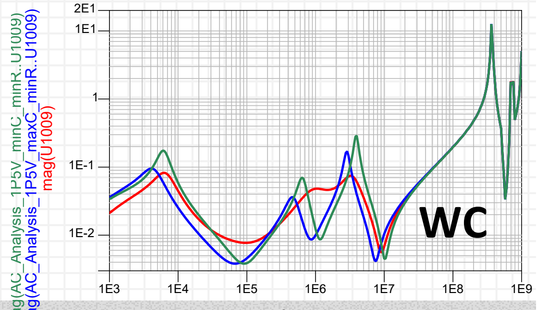
Power Supply IC Manufacturers

Power Supply Designer



Where does the responsibility lie?

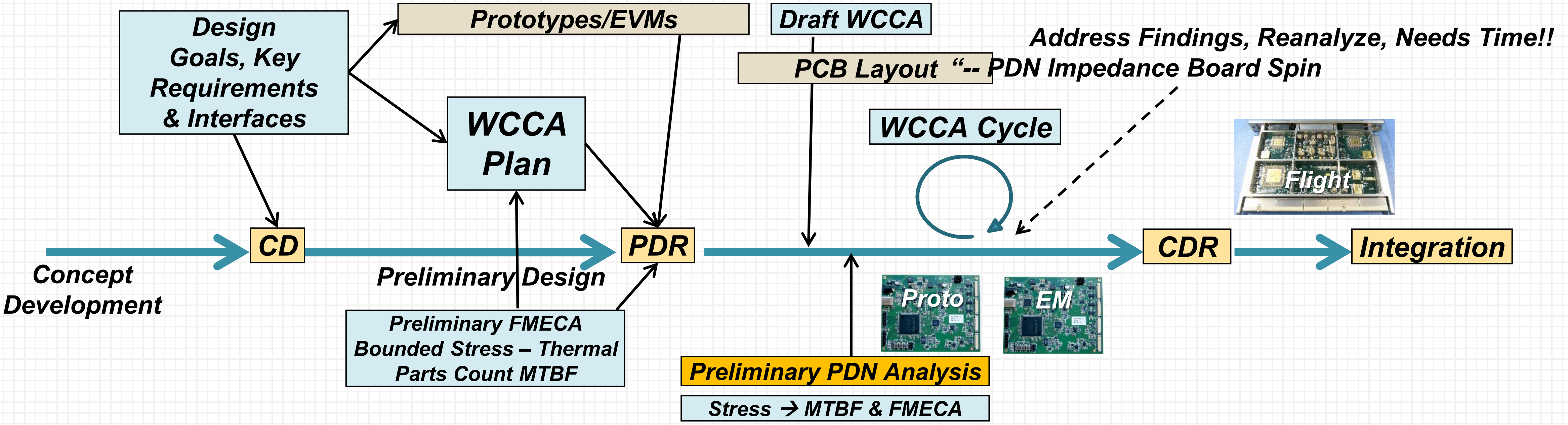
Digital Load/Software Designer



PS Impedance = Plane/load Impedance

Schedules Still Not Right

What is the cost trade-off of analysis vs. test? An extra board spin!



- Proper scheduling is essential to meeting target impedance
  - The performance of FPGAs, CPUs, and other high-speed logic devices is directly dependent on the PDN
- No where is simulation more essential then in Power Integrity
  - Testing is very challenging
  - Dynamic currents are unknown - 3D FEA to include PCB effects is essential
- Even with analysis, a board spin is almost always desirable/necessary

PDN Recommendations Still Stand

- Learn how the power supply interacts with the system and the load
- Establish a noise budget
- Set the VRM target impedance from the noise budget
- Design the VR
- Learn to interp s
- Don't design u
- Put pressure c de complete high-quality data
- **MEASURE - MODEL - ANALYZE – BUILD - TEST - ANALYZE – BUILD**
  - Sorry if you thought it was just TEST → BUILD → SHIP

We Are Hurting Ourselves

We are not asking the difficult questions

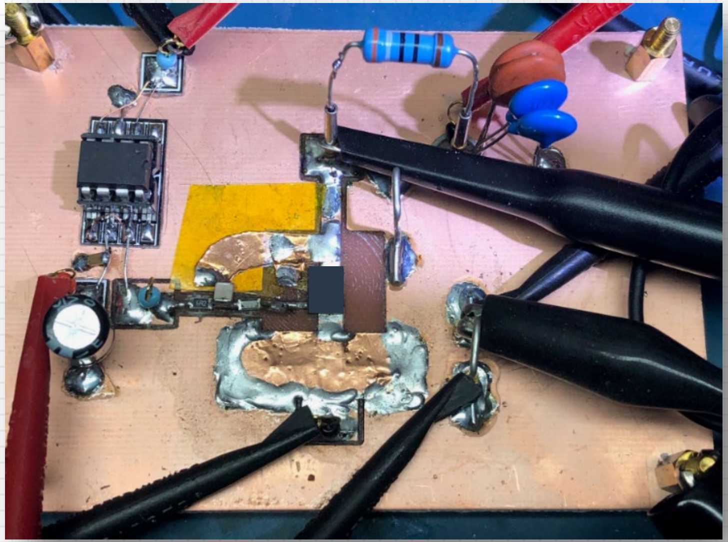
Zero planning or thought about flat PDN impedance

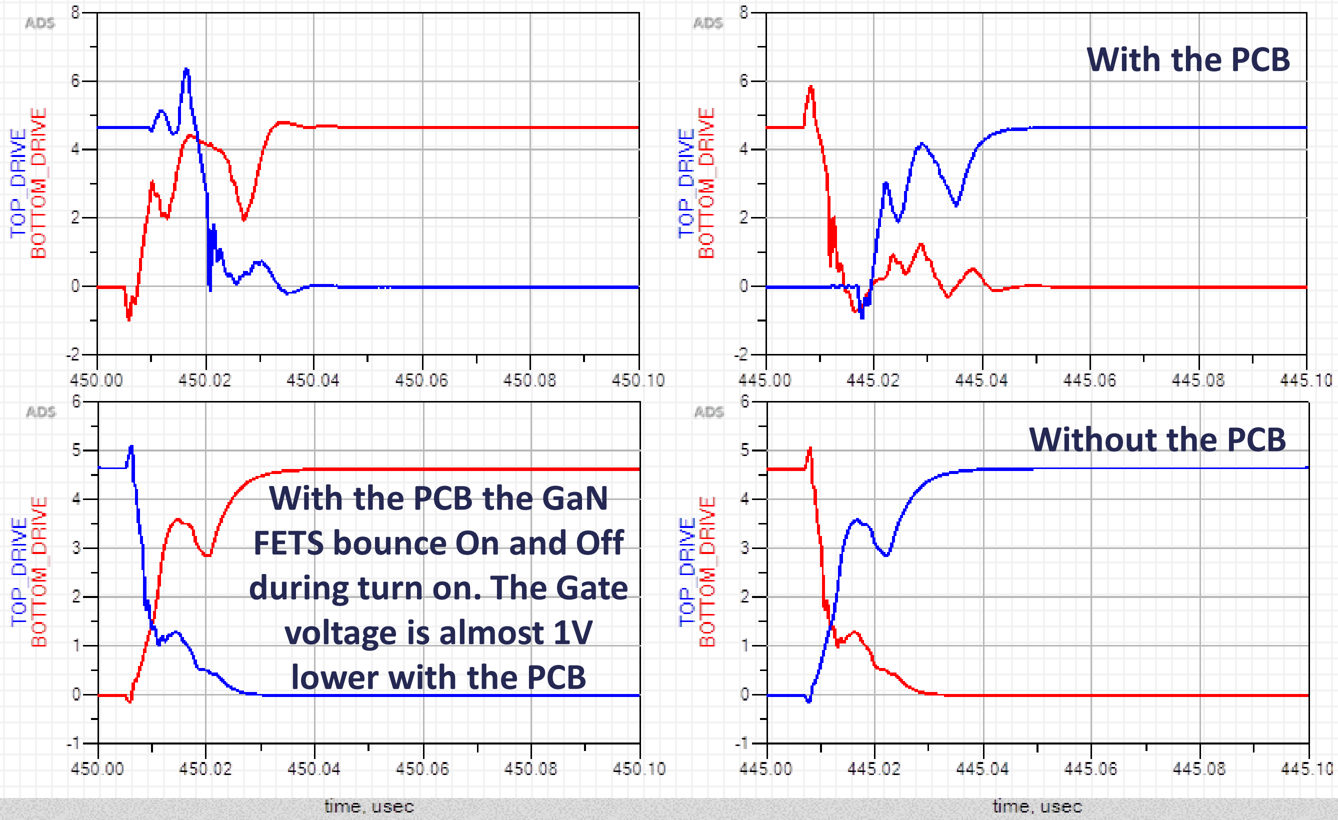
Zero assessment (Simulation/Test)

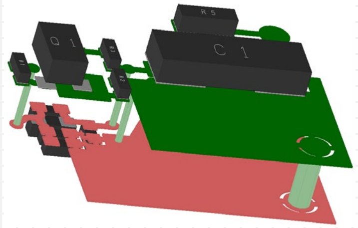
Not enough time/money for multiple iterations

It's About to Get Tougher Still

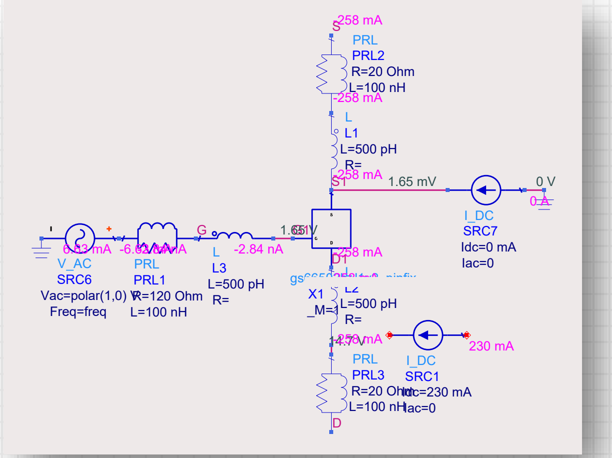
- GAN Design requires EM sims
- Inclusion of the PCB
- Parasitics, Measurements to make models







GAN FET self-oscillated
Needed beads to tame



Closing Slide and Call to Action

- **Wake up – Power Integrity is a thing**
- **MEASURE - MODEL - ANALYZE – BUILD - TEST - ANALYZE - BUILD**
- **Space Power needs to make this a <u>permanent</u> track**
  - There isn't another forum, and the industry is suffering

References

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10. The 5-Minute Method for Stabilizing Any Control Loop, Steve Sandler, January 28, 2020

Submitted Abstract

PMAD – Power System Design and Analysis
Power Integrity Challenges In the Space Industry, An Update

Abstract: Many changes in technology have occurred since I started in the Space Power Electronics, working on the Space Shuttle program, in the 1970's. Certainly, both the systems and the power electronics were much simpler. Today's systems demand much better performance, power systems are complex, rad-hard FPGA's have tight power integrity requirements and many power rails are often used, placing greater emphasis on the assessment and optimization of power electronics.

Since the last presentation on Power Integrity at Space Power 2017 we've seen a dramatic increase in the number of worst case analysis findings related to power electronics and power integrity. We see many issues, but two of the most common are:

1. Startup. Overshoot of the voltage regulators exceeds the absolute maximum voltage rating of the sensitive, and very expensive FPGA's. This is, in large part, due to the lack of a soft-start circuit in the voltage regulator.
2. Stability issues are also quite prevalent, due to the expanded use of multiple nested control loops in the voltage regulator, particularly in the linear regulators and LDOs.

To be fair, designers are doing their part to assess and analyze their designs properly, though increasingly, the vendor provided simulation models are incomplete, unvalidated, and in most cases just plain wrong. Many of these parts are older, the designers are long gone, and vendor support isn't familiar with the inner workings of the part. The lack of an accurate model has unfortunately not stopped designers from using them, unaware of the inaccurate results or hamstrung with no other path.

In order to reduce the number of worst case analysis (and system performance) failures it is essential that these voltage regulators be fully characterized, and any simulation models used need to be validated against the measured data.

Topics to add

- TPS7A4501 – vendor correlated the Bode plot not the output Impedance so the stability prediction is wrong
- Differences between pspice and simplis output impedance Intersil model
- ISL75051 low inductance requires PCB to get the right answer
- Moog bead destroys PDN

- SPI-2017