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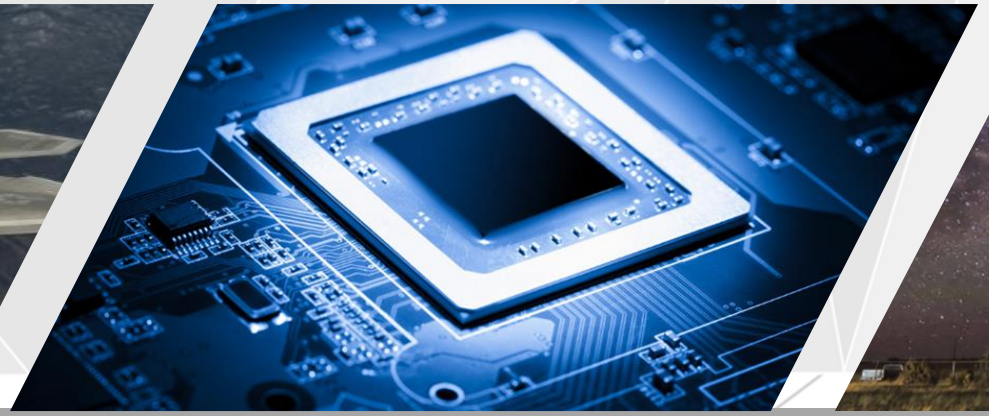
ALPHACORE
ROBUST HIGH-PERFORMANCE MICROELECTRONICS

A Novel Dynamic Solar Array Reconfiguration Capability for Spacecraft Power Systems

Space Power Workshop
April 2021


Agenda: Dynamic Solar Array Reconfiguration

- Motivation and Solution
- System Architecture
- Technology Overview
- CMOS ASIC Design, Layout and Packaging
- CMOS ASIC Measurement and Analysis
- COTS Test Board Development and Measurement
- Next Steps
- Conclusion

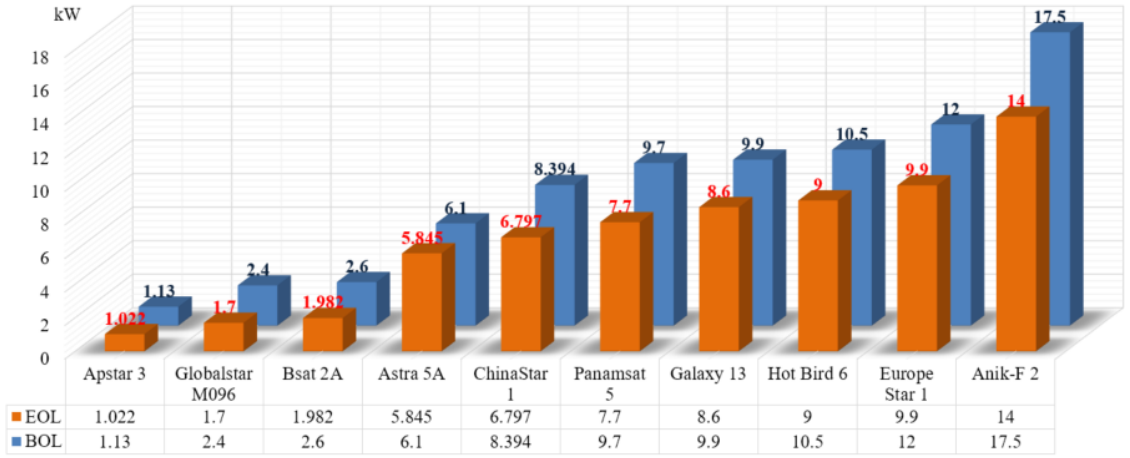
Many thanks to co-authors and team members:
- Alphacore: Dr. Yu Long, Eric Weeks, Ted Olivarez
- Arizona State University: Anand Heblikar, Dr. Jennifer Kitchen, Dr. Sule Ozev
- Boeing Spectrolab: Dr. Eric Rehder

Motivations for Solar Array Interface

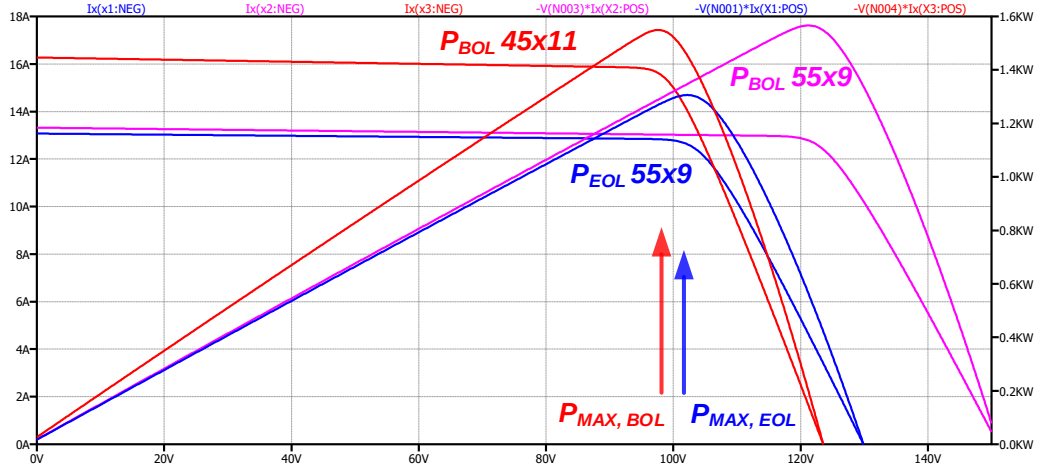
- Solar arrays can degrade from 20% to 50% in power producing capability over a 15-year mission. 10-50% of the spacecraft power is wasted during the beginning of life(BOL).
- Current spacecraft power systems are not capable of re-allocating power to different loads.
- Reconfiguring the array over its lifetime may allow for significant increase in power extraction over spacecraft lifetime:
  - BOL at 45×11 and EOL at 55×9 shows improved power delivery and stable power bus over lifetime

		V_{OC} (V)	I_{SC} (A)	V_{MP} (V)	I_{MP} (A)	η (%)
BOL	Datasheet	2.750	1.488	2.435	1.424	32.2
	Simulation	2.745	1.485	2.420	1.422	32.0
EOL	Datasheet	2.365	1.458	2.094	1.396	27.0
	Simulation	2.361	1.456	2.069	1.405	26.8

Datasheet and simulated values for XTE_SF solar cell (80cm^2), EOL: 15 years GEO, TID 1E15 @ 1MeV electron/cm^2 fluence

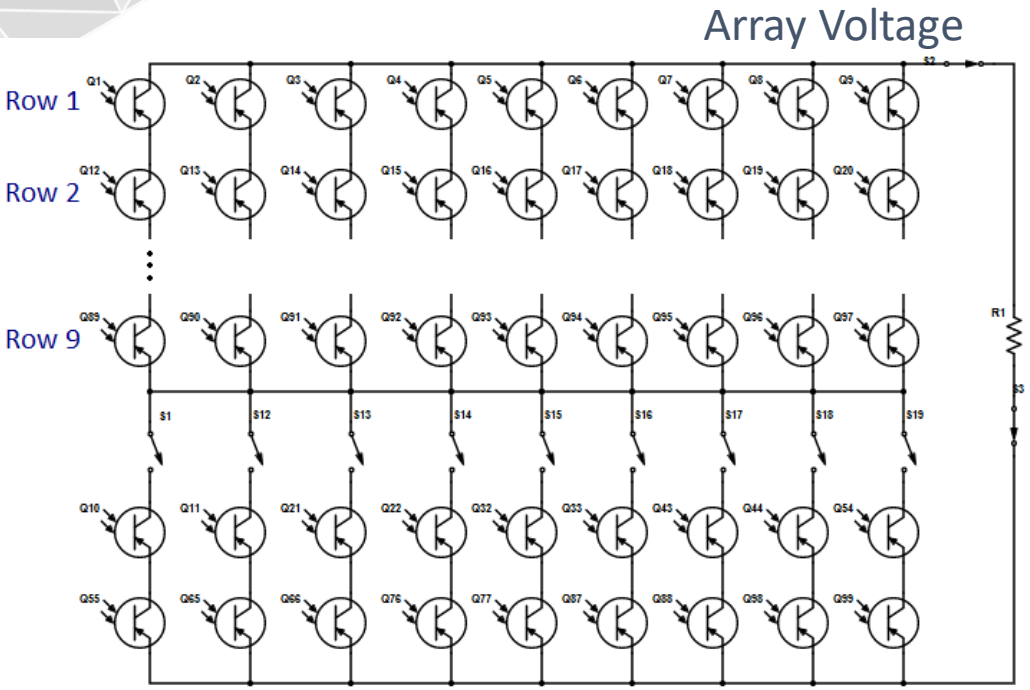


Selected satellites power generation at BOL and EOL

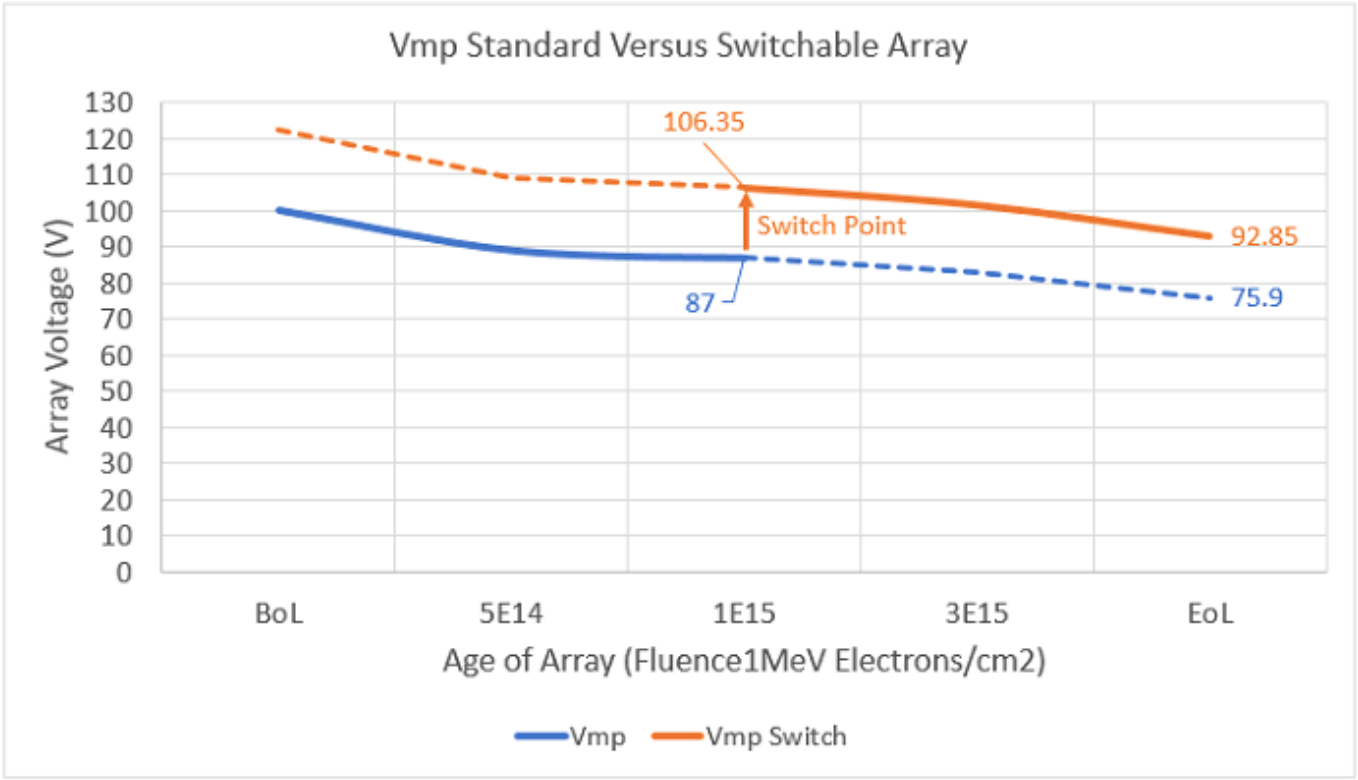


Simulated I-V, P-V curves for XTE_SF solar cell, 80cm^2 at BOL (55X9, 45X11)) and EOL (55X9)

Solution: Dynamically Reconfigurable Array

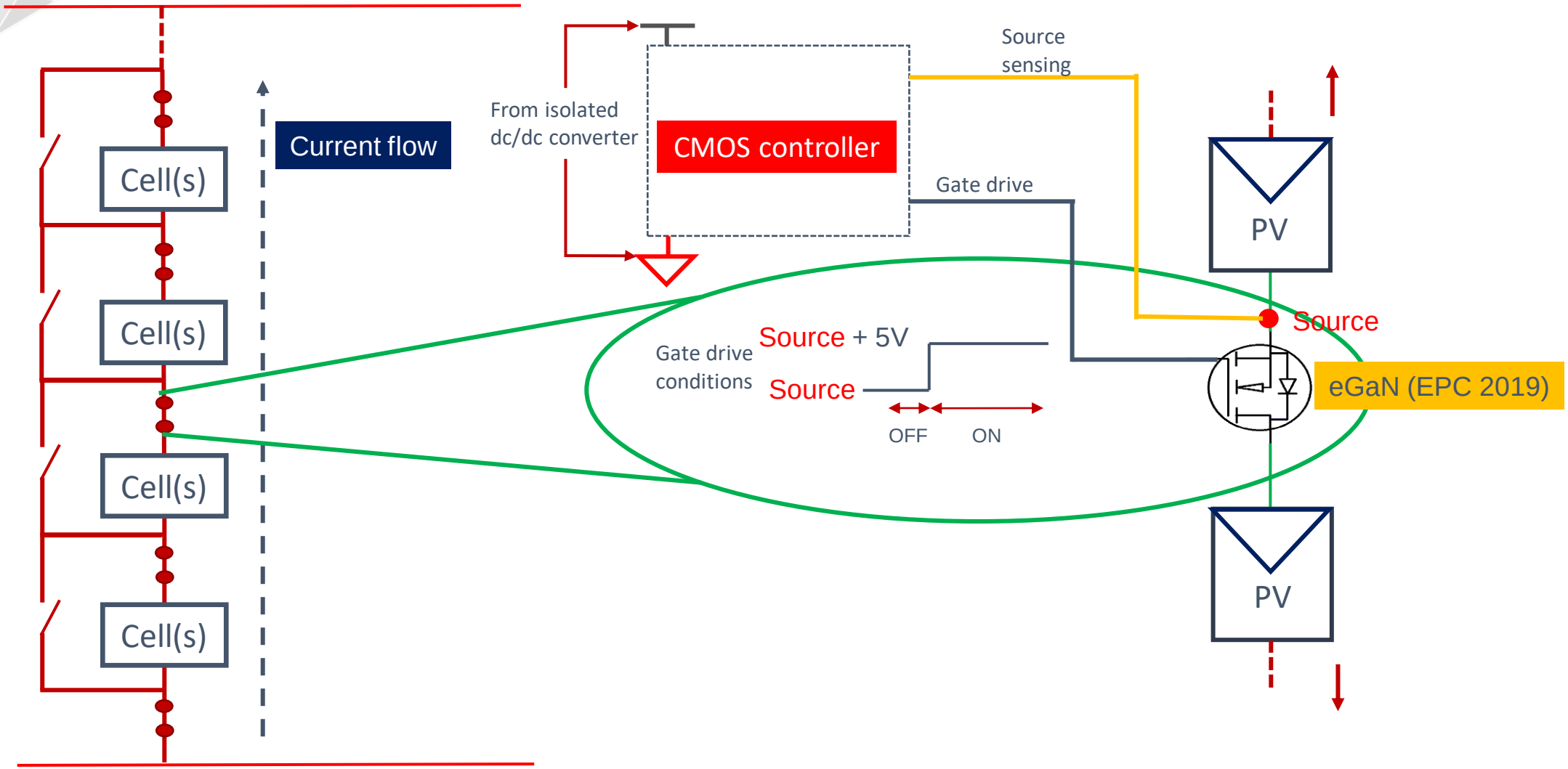


Switch cells in and out of columns to reconfigure for: different output voltage, various loads, and solar cell performance degradation.



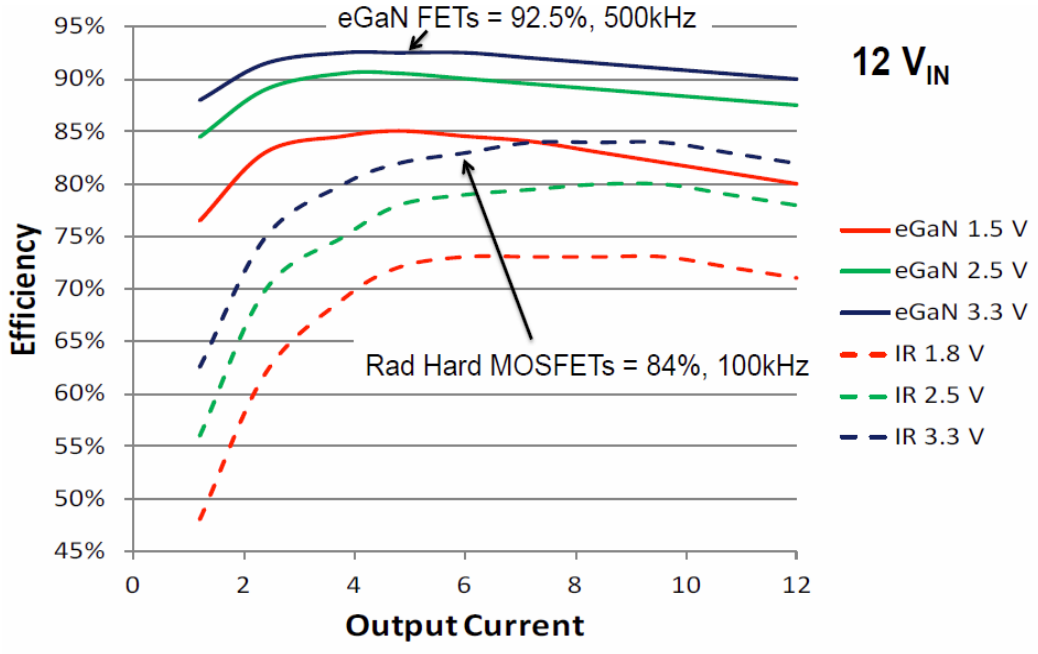
Array output voltage with aging (irradiation). The output voltage degrades with time and switching the array configuration can recover output voltage.

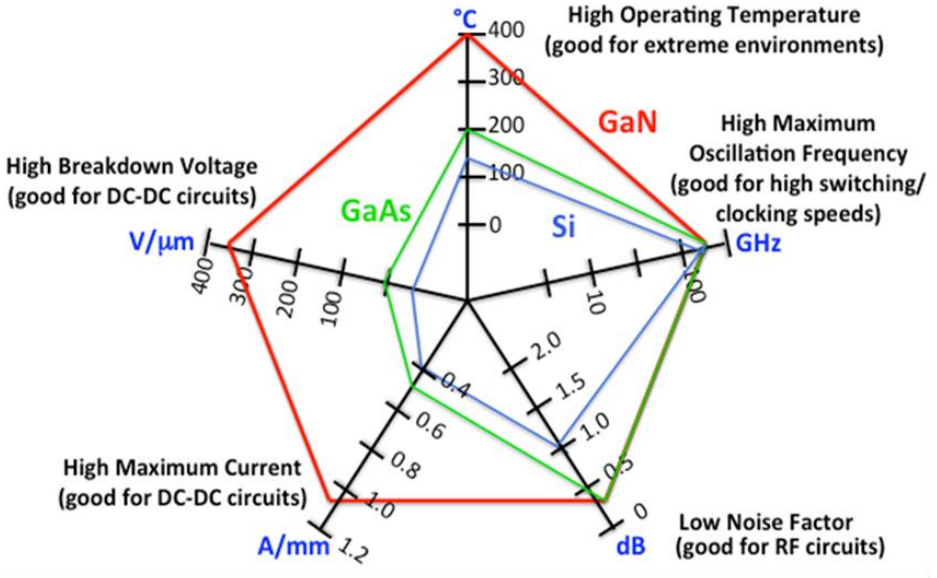
The Switch and CMOS Controller

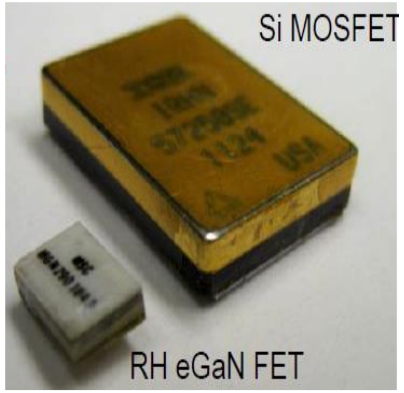


Switch Hardware: Why GaN?

- **Low on resistance (RON)**
- **Small footprint**
- **TID hard**



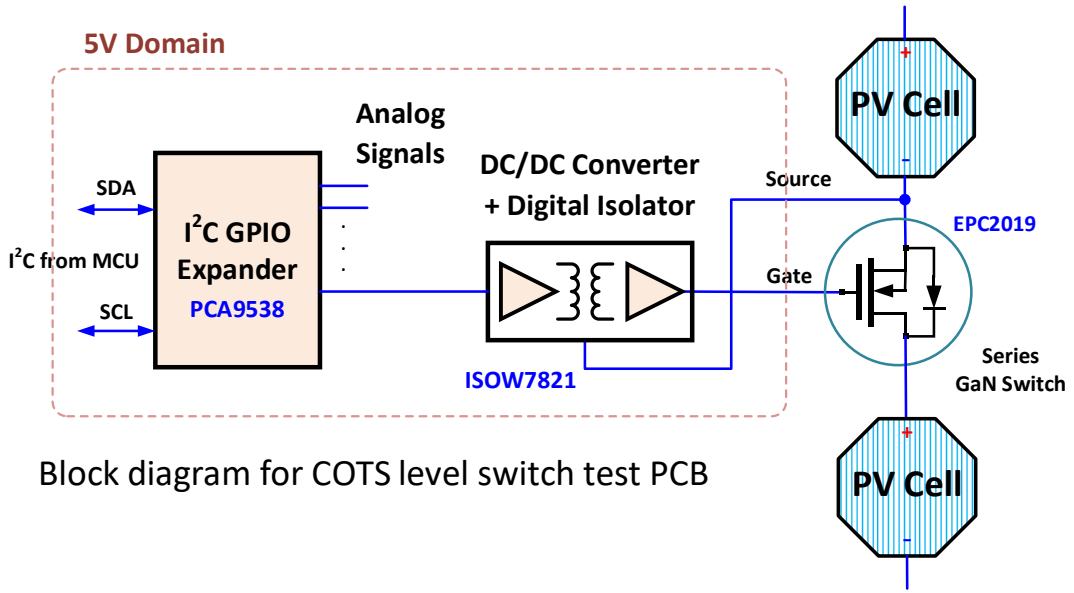




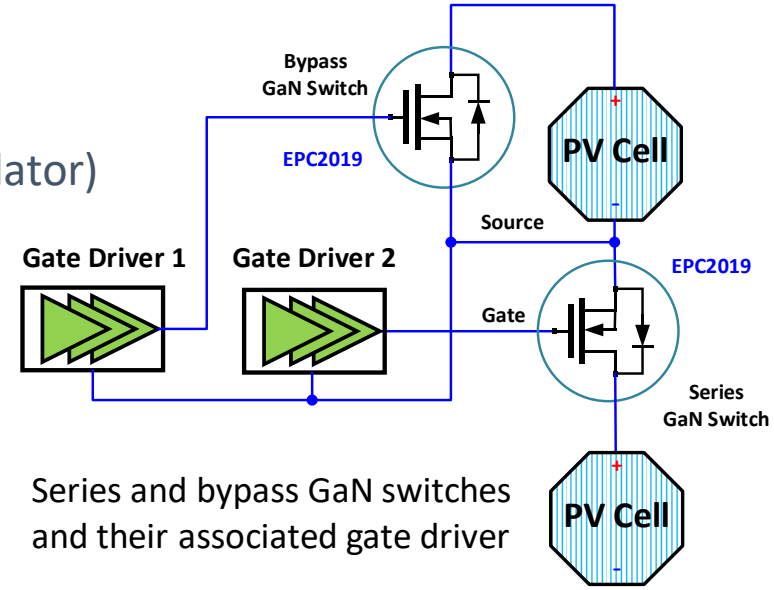
Source: GaN Systems

Solar Array Switch and Driver Architecture

- Floating voltage challenge: Gate drive should dynamically read the source voltage and provide correct gate drive voltage.
- GaN has maximum gate-to-source voltage limited to ~5V, GaN switch driver can be:
  - Transformer based (board implementation)
  - Capacitive based (integrated circuit implementation)
- COTS I^2C expander IC and isolated DC/DC supply IC (integrated with signal isolator) to implement signal transfer and isolated power supply.



Block diagram for COTS level switch test PCB



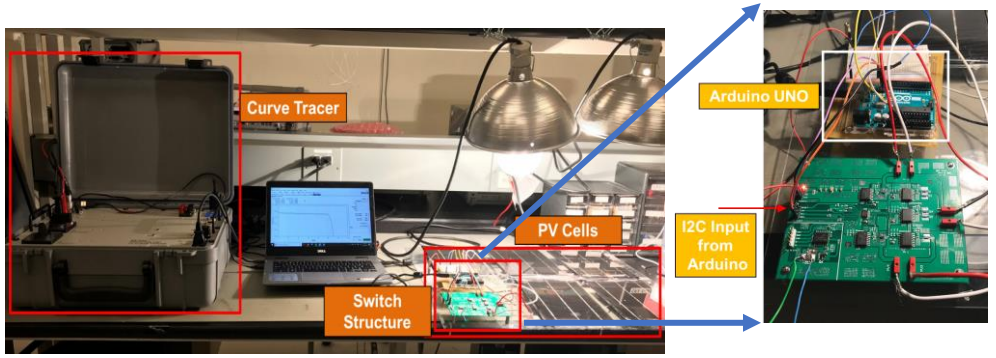
Series and bypass GaN switches and their associated gate driver

- Series and bypass GaN switch have different drain-source connections based on On/Off operations requirements

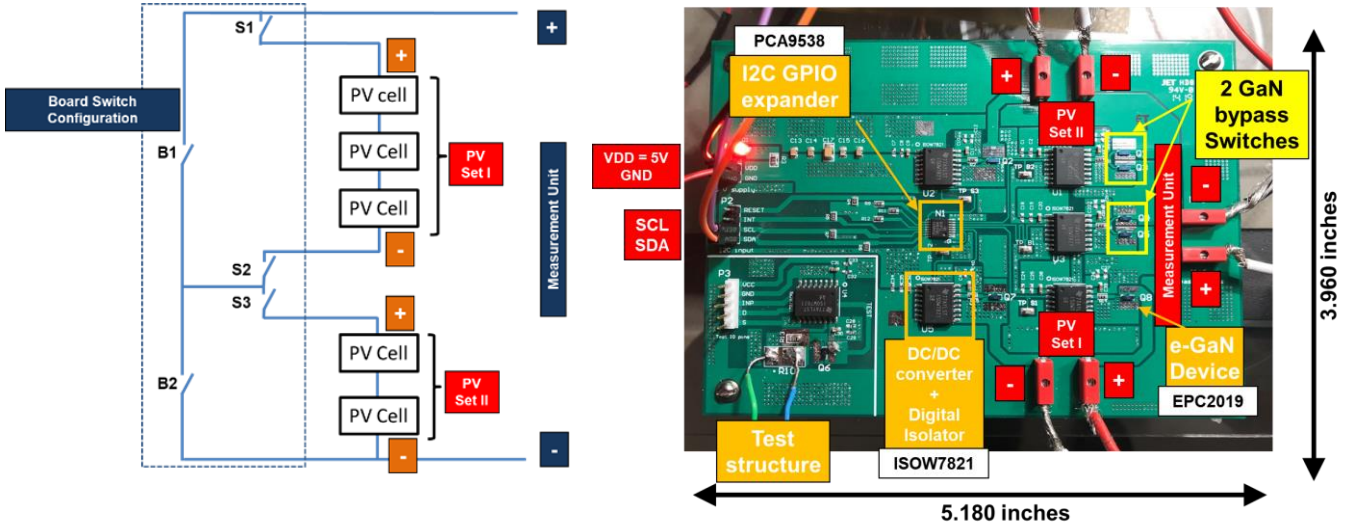
Discrete COTS Level Prototype PCB Testing

- A protype PCB with discrete COTS components built to verify the functions of solar panel GaN switch control.
- Series and bypass GaN switch implemented to switch the array connections
- Simulation and measurement demonstrate the effective of the dynamic switch control.

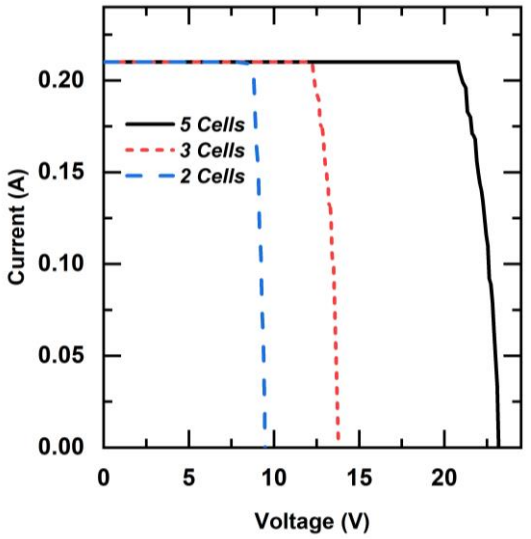
Testbench setup



COTS solar array control prototype PCB and its panel control configurations



Measured solar panels I-V output curves with series GaN switches controlled by prototype PCB

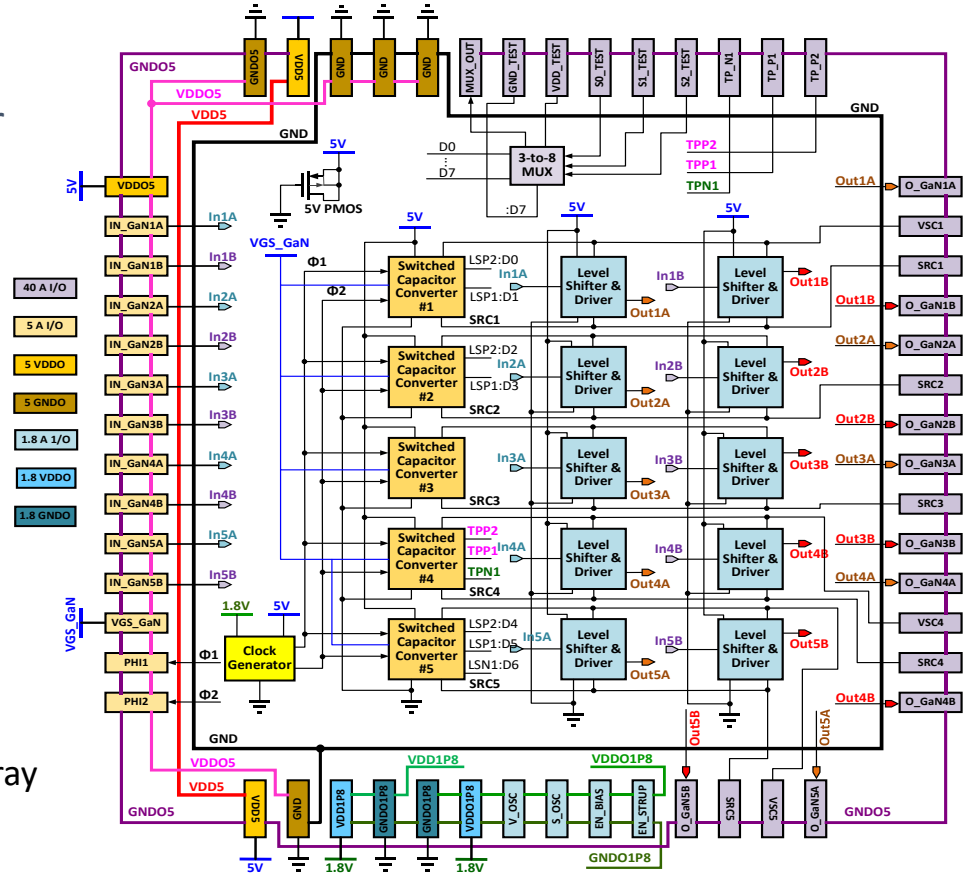


Switch Controller CMOS ASIC Architecture and Design

- Power supply: 1.8V, 5V, Switched capacitor supply input: ~5.5V (could be shared)
- 10 independent switch control inputs, 5 output pairs (each pair shared source node)
- 5MHz internal clock, optional external clock, built-in testing circuit to probe key node voltages
- 180nm commercial high-voltage SOI process
- Radhard SOI CMOS process and GaN power transistor

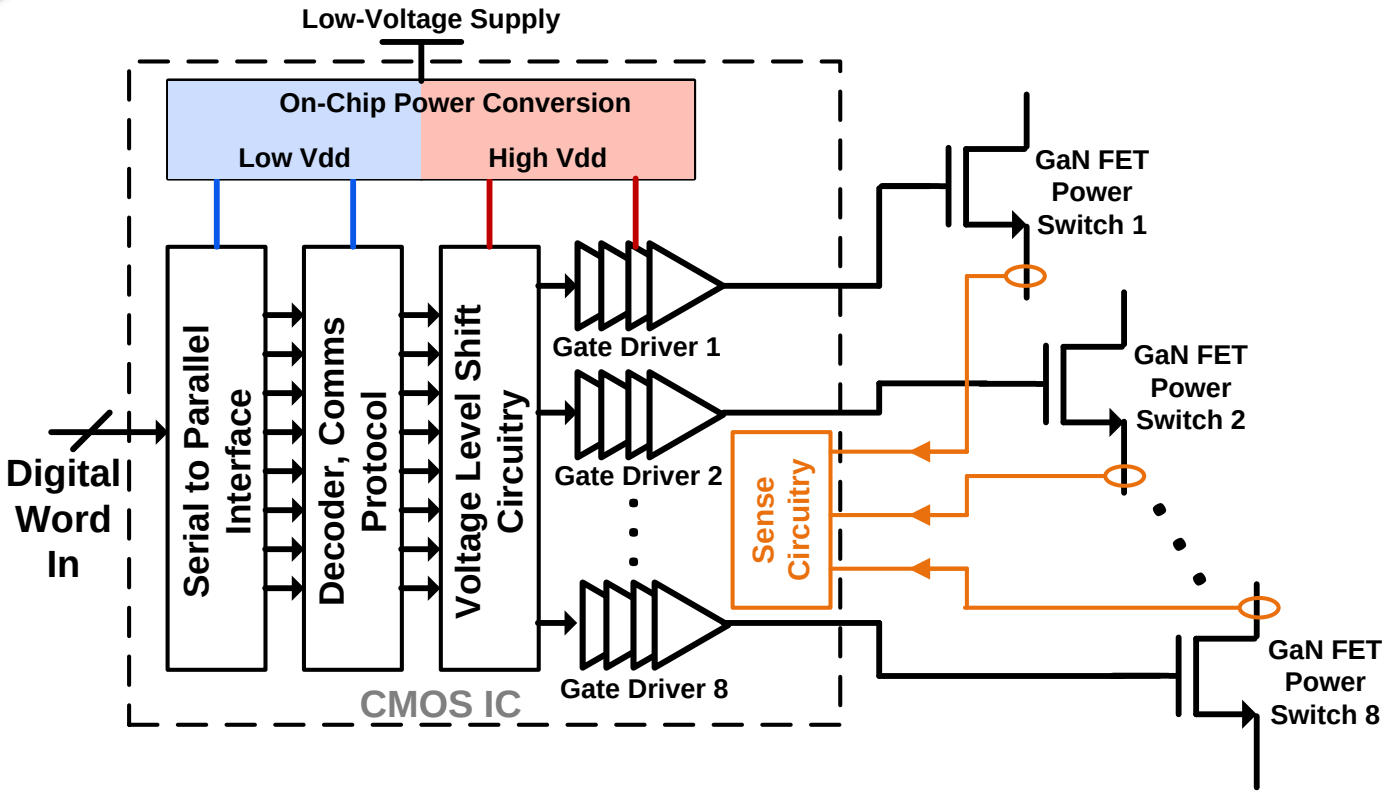
Key design specifications

Output bus voltage	30V max	Fringe capacitor breakdown voltage
Output current	8.5A	One solar cell string, EPC2019
Switch on resisrance	50mΩ	EPC2019
Response time	< 5µs	Delay from IC input to output
Switch-on loss	<0.11W	One switch for one cell (1.424A)
Efficiency	>96.8%	One switch for one cell (1.424A, 2.435V)



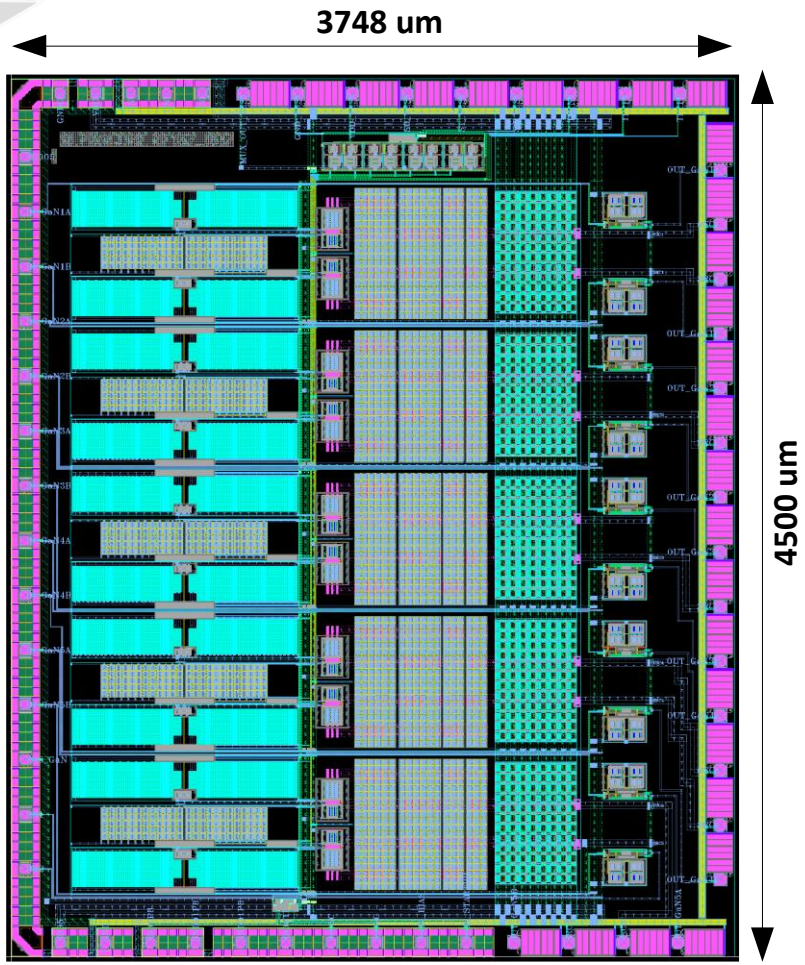
Top-Level architecture for solar array GaN switch control IC

CMOS-GaN Switch Module



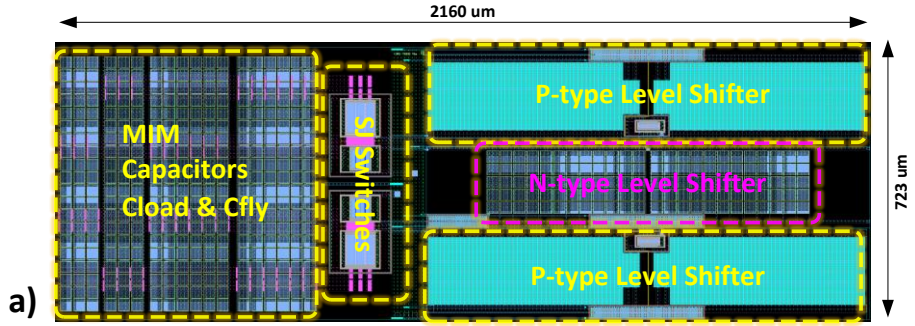
- Controller IC must isolate the MCU (digital input) from the high-side drive voltages
- The drivers must provide a floating signal control, with reference to each switch's source
- A single CMOS ASIC should control multiple (e.g., 5-10) GaN switches

Switch Controller ASIC Design and Layout

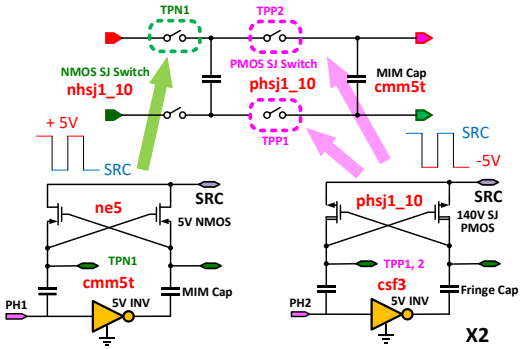


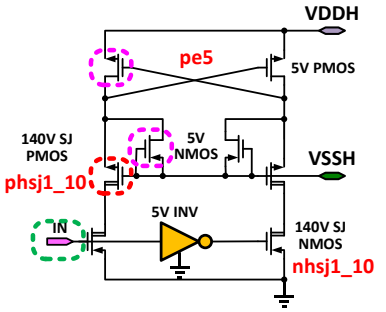
Top layout view with bonding pads

- 1.8V CMOS for digital circuits, 5V for GaN gate drive circuits, 100V SJ DMOS for high voltage operation
- MIM capacitors used for 5V operation, fringe capacitors for clock shifter isolation, SJ DMOS for high voltage signal shifting
- Separate I/O pads for different voltage level signals
- No radhard ELT layout used, development in progress with projects

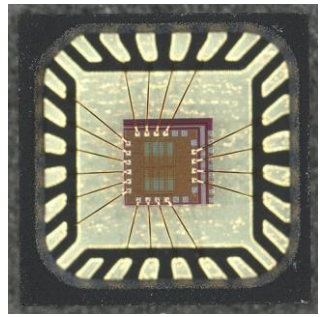


Key circuit blocks: a) switched capacitor power supply, b) level shifter and gate driver

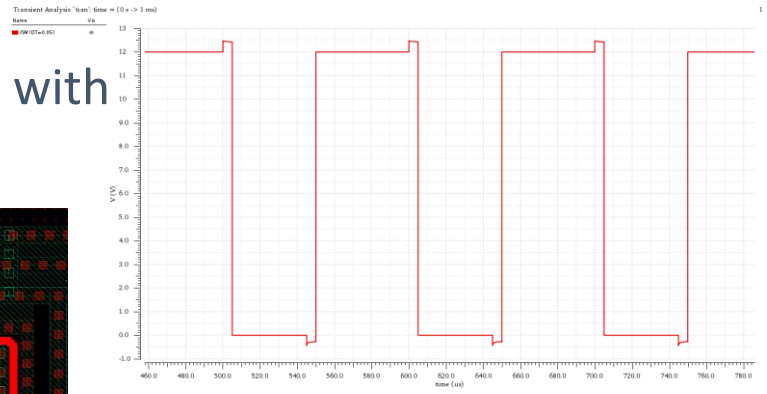


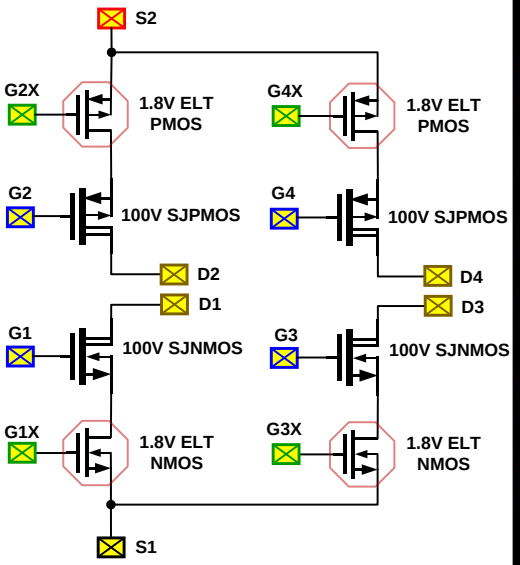


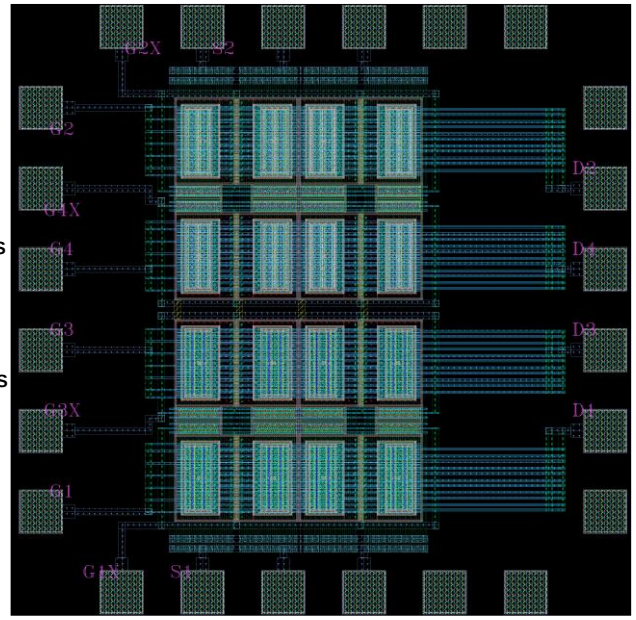
Rad-Hard by Design (RHBD) Techniques

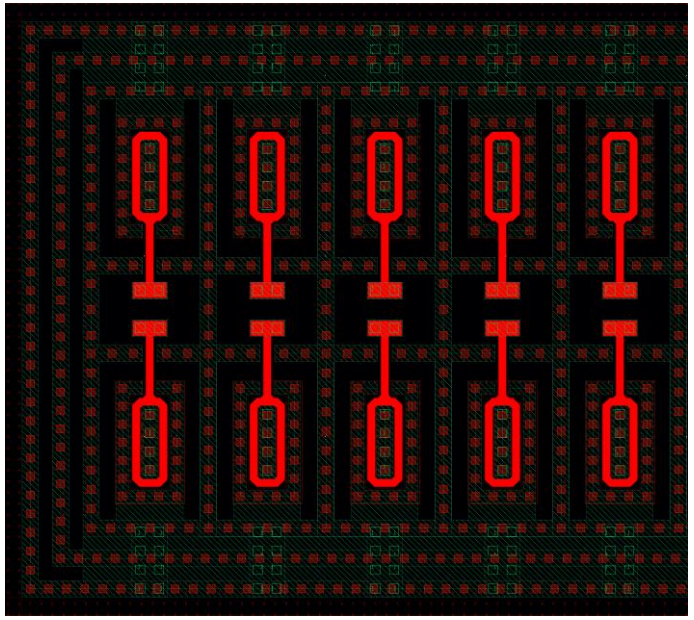


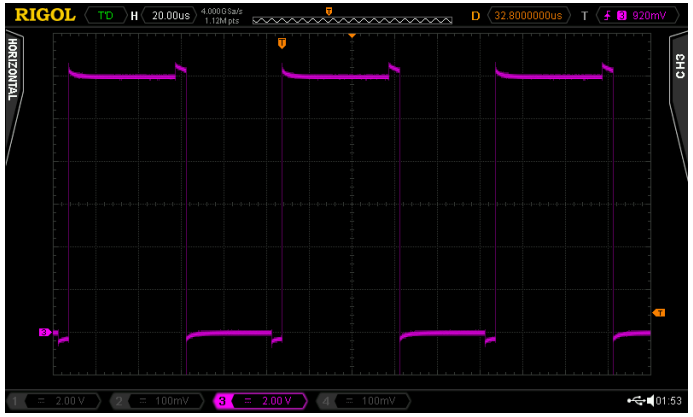
- We designed rad-hard enhanced layout transistor (ELT) for 1.8V and 5V
- All custom ELT devices are DRC & LVS clean, placed and simulated as normal PDK instances
- Extensive and maximum guard rings, body rings and isolation rings used
- Measurement shows expected operation of custom ELT devices integrated with 100V SJ DMOS







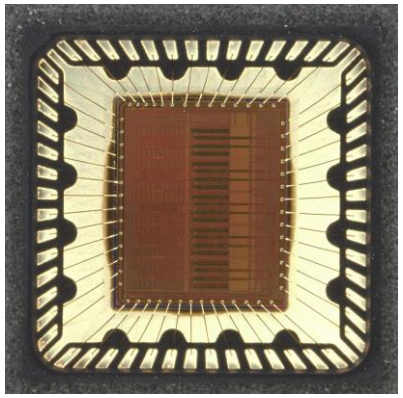




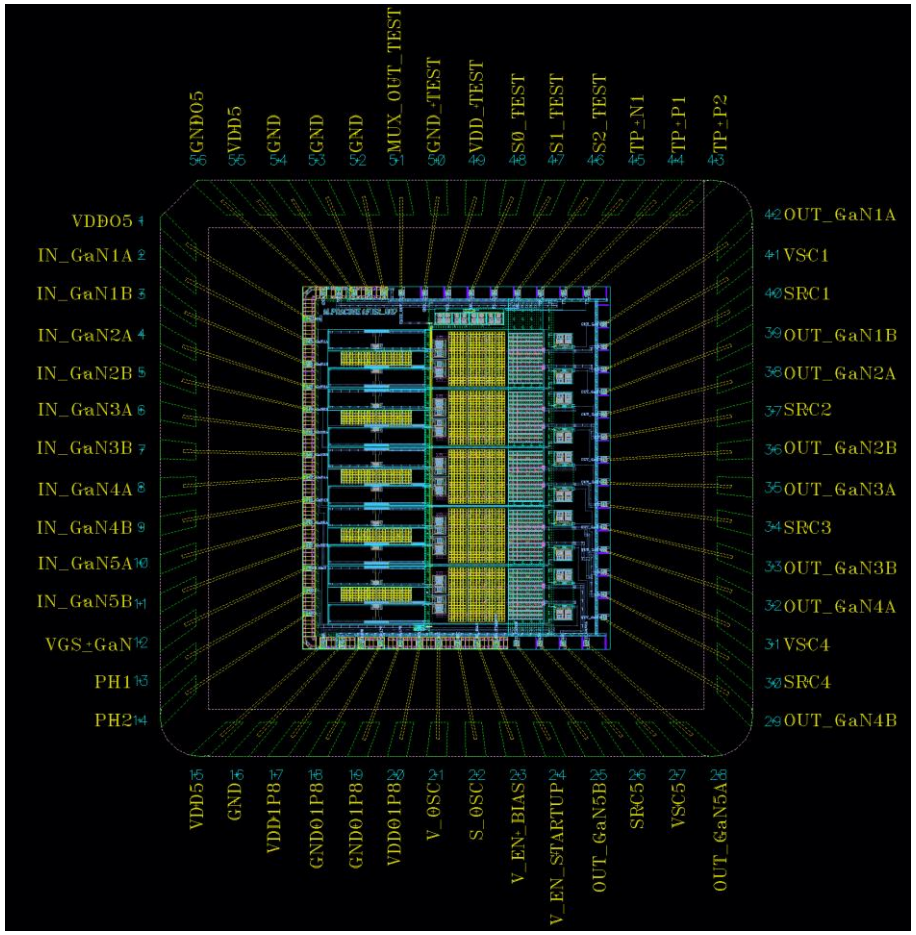
Controller ASIC Bonding and Packaging

- Library I/O pads with ESD
- 5V and 1.8V analog I/O pads
- 40V analog high-voltage I/O pads
- 56-pin standard QFN56 (8mm × 8mm)

QFN56 package



Bonding diagram

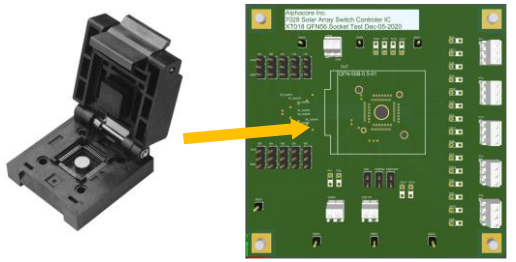


Pin assignment and bonding pads selections

#	Pads Name	Power	Ground	Pad	Number	Descriptions
1	VDDO1VPADNF	VDDO1P8	GNDO1P8	VDDO1P8	1	1.8V VDDO power supply pad
		VDD1P8		VDD1P8	1	
2	GNDO1VPADNF	VDDO1P8	GNDO1P8	GNDO1P8	1	1.8V GNDO ground supply pad
		VDD1P8			1	
3	VDDO5VPADNF	VDDO5	GNDO5	VDDO5	1	5V VDDO power supply pad
		VDD5		VDD5	2	
4	GNDO5VPADNF	VDDO5	GNDO5	GNDO5	1	5V GNDO ground supply pad
			GND	GND	4	
5	AP1VNR00BF	VDDO1P8	GNDO1P8	1.8V I/O Signal	4	1.8V analog I/O <1Ω series resistance
6	AP5VNR00BF	VDDO5	GNDO5	5V I/O Signal	13	5V analog I/O <1Ω series resistance
7	HVP4J6PM	N/A	GNDO5	30V I/O Signal	27	40V latch-up robust analog I/O

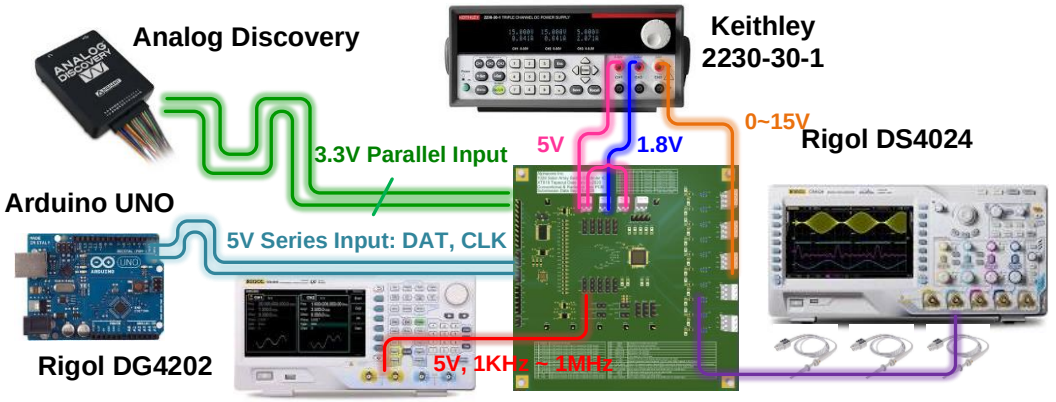
CMOS ASIC Functional Test

- An IC test PCB built with the custom GaN switch controller IC
- Control IC power supply: 1.8V, 5V (shared w, VGSIN), GaN switch shifted reference: 0~6V
- Signal generator direct pulse input for I/O functional verified
- Programmed input options verified:
  - Parallel input by coded Analog Discovery, Series input by programmed Arduino UNO
- Another test PCB with QFN56 socket to select IC without soldering on board



QFN56 socket-based test PCB

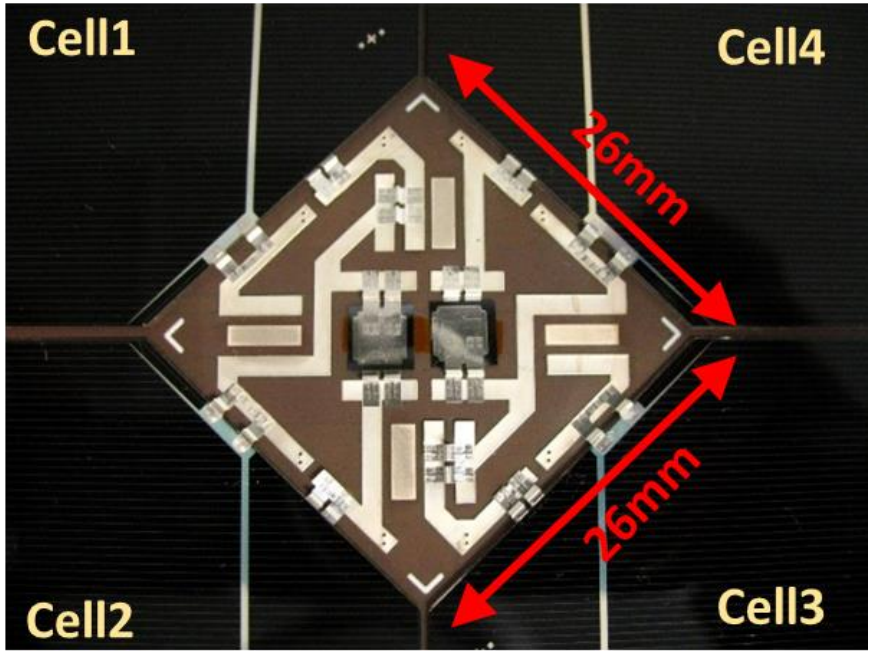
Custom GaN switch controller IC prototype PCB test setup

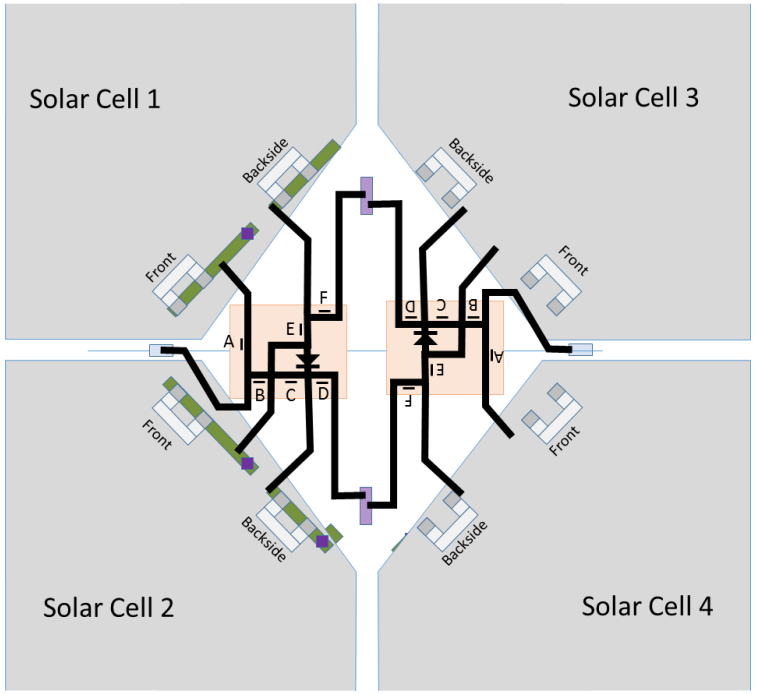


IC output test results shows significant performance variation

IC	PH1	PH2	SC1	G1A	G1B	SC2	G2A	G2B	SC3	G3A	G3B	SC4	G4A	G4B	SC5	G5A	G5B
P1	E	E	P	P	P	G	G	G	P	P	P	G+	G+	G+	G+	G+	G+
P2	E	E	P	P	P	P	P	P	G	G	G	P	P	P	G	G	G
P3	E	E	G	G	G	G	G	G	P	P	P	G+	G+	G+	G+	G+	G+
P4	E	E	P	P	P	G	G	G	P	P	P	P	P	P	G	G	G
P5	E	E	G+	G+	G+	G	G	G	G	G	G	G+	G+	G+	P	P	P
P6	E	E	P	P	P	P	P	P	G	G	G	P	P	P	G	G	G
P7	E	E	P	P	P	G	G	G	P	P	P	G	G	G	G	G	G
P8	E	E	P+	P+	P+	G	G	G	G	G	G	P	P	P	G+	G+	G+
P9	E	E	G	G	G	G+	G+	G+	G	G	G	G+	G+	G+	G+	G+	G+
P10	E	E	G	G	G	G	G	G	P	P	P	P	P	P	G+	G+	G+

Solar Cell Array Tile with Integrated Switch Module: Spectrolab Collaboration

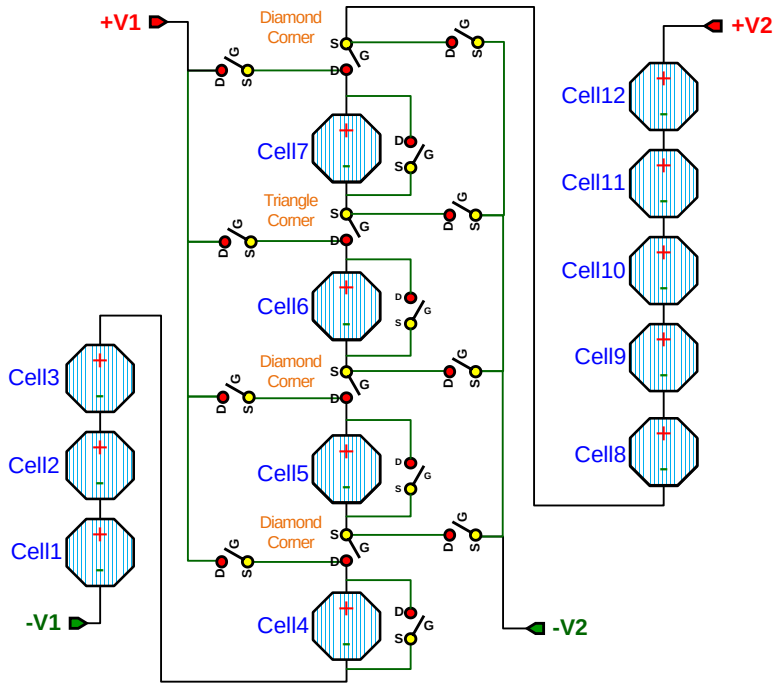




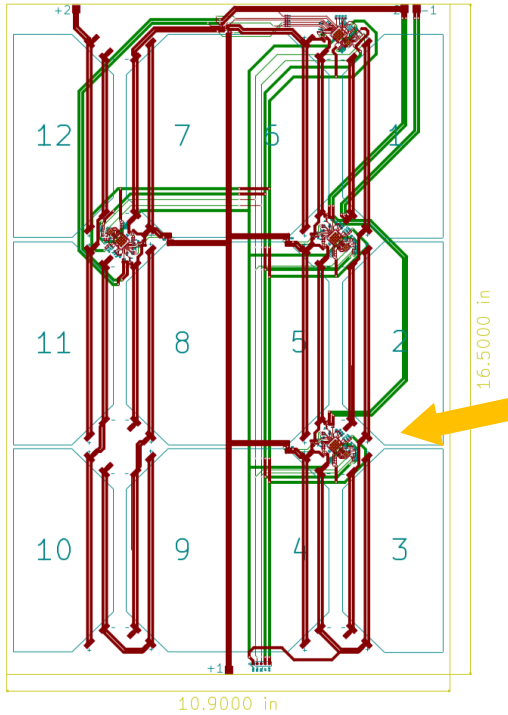
- Alphacore's switch module must integrate within this solar array "tile" developed by Spectrolab.
- Tile size is ~26mm x 26mm. All switches and controller for a minimum of 4 cells must fit within this area.
- Other applications for a rollup array would require the switch module to be split into two triangle shapes to accommodate a folding flex sheet.

Flex Circuit Design for Spectrolab

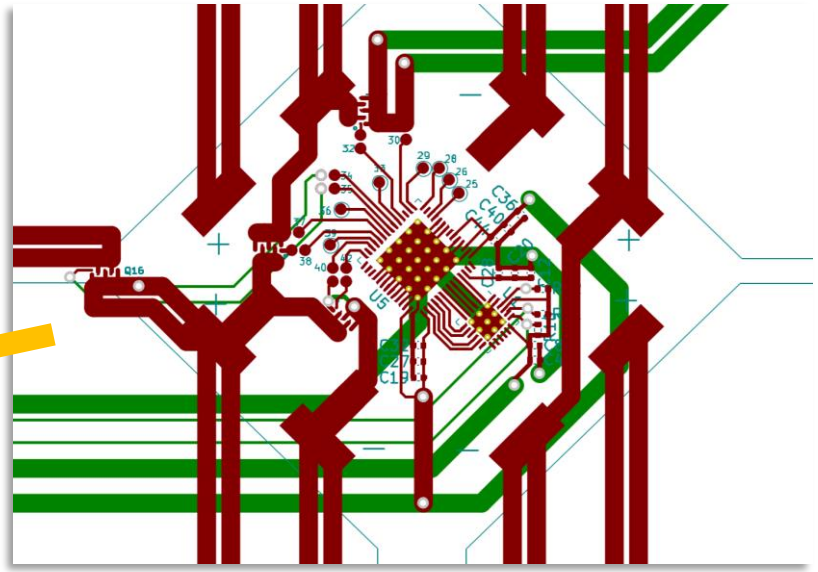
- Total 16 switches, each functional IC provides up to 5 independent switch control.
- 4 switch control ICs to be used on Flex PCB for test at Spectrolab
- Each IC will have 4 selected switch output verified as **Good**



Solar panel switch connection topology



Array layout with 4 controller ICs



Zoom-in layout view of one controller IC at corner of 4 neighboring solar panel

Next Steps

Current Phase II Program

- Transfer conventional PCB design to flex circuit board
- Integrate into solar panel at Spectrolab
- Test the integrated system for basic functionality
- Temperature cycle the integrated system
- Test the Controller ASIC for radiation hardness

Beyond Phase II

- Upgrade and optimize the CMOS ASIC
- Upgrade and optimize the switch control module
- Engage with spacecraft integrators for technology transition

Conclusion

- The need for solar array reconfiguration was defined.
- A prototype board was fabricated to verify the topology of solar array reconfiguration
- A compact and low-mass silicon-based CMOS-integrated GaN controller was designed and tested.
- Functional tests shows effectiveness of the proposed architecture and designs.
- Controller ASICs with Flex Circuit test for solar panel array will be conducted.
- Planned CMOS ASIC controller revision will improve the circuit design and layout, and reduce performance variation.
- Further work will result in a high TRL module ready for qualification.

Thank You!

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